Lecture #6 : Single-ended stage and differential pair

1. **Single-ended stage**
   - o General description
   - o Small-signal model of a bipolar transistor
   - o Small-signal model of a MOSFET transistor
2. **Differential pair**
   - o DC transfer characteristic
   - o Small signal characteristic
   - o Improvement of CMRR
   - o Increase of voltage swing
   - o Interference cancellation
   - o Increase of noise
3. **Apparent difference between single ended stage and differential pair**
4. **DC offset**
   - o DC offset in a single ended device
   - o Zero DC offset in a pseudo differential pair
   - oWhy "zero" IF or direct conversion
   - oDC offset cancellation

1. Single-ended stage

o General description

* Voltage gain and current gain of a device in low frequency

Table 6.1 Voltage gain and current gain of a bipolar and CMOS device in low frequency. **($Z_{L,A}$=Actual load impedance)**

Configuration	Voltage gain	Current gain	Z_L
CE	$-g_m(r_o // z_L)$	b_o	$z_L = R_C // z_{L,A}$
CB	$g_m z_L$	a_o	$z_L = R_C // z_{L,A}$
CC	$\dfrac{(b_o+1)\dfrac{r_o z_L}{r_o+z_L}}{r_b+r_p+(b_o+1)\dfrac{r_o z_L}{r_o+z_L}} \to 1$	$(1+g_m r_p)\dfrac{r_o}{r_o+z_L} \to (1+b_o)$	$z_L = R_E // z_{L,A}$
CS	$-g_m(r_d // z_L)$	$\to \infty$	$z_L = R_d // z_{L,A}$
CG	$(g_m+g_{mb})z_L$	$\to 1$	$z_L = R_d // z_{L,A}$
CD	$\dfrac{g_m r_d}{1+(g_m+g_{mb})r_d+\dfrac{r_d}{z_L}}$	$\to \infty$	$z_L = R_S // z_{L,A}$

o General description (Continued)

* **In the cases when the RF circuit is operating in RF frequency range or the digital circuit is operating with high data rate,**

  - ***Either voltage or current gain is less important than power gain. Power transportation must be considered as the first priority.***

  - ***The power gain is mainly determined by the performance of input and output impedance matching. The designers very concern the input and output impedances in a variety of configurations,***

  - ***A basic single ended amplifier can be demarcated into 3 portions.***

It is therefore concluded that the study of input and output impedances of a device, Z_{in} and Z_{out}, with different configuration becomes prerequisite.

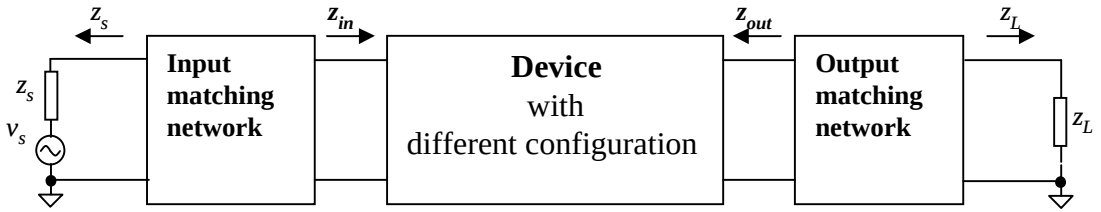


Figure 6.1 A basic single ended amplifier can be demarcated into 3portions.

- ***Example #1: a LNA***

  a) Input impedance matching
  b) Output impedance matching
  c) Low noise
  d) Power gain

- ***Example #2: a buffer after VCO***

  a) High input impedance , unmatched
  b) With power gain
  c) Output impedance matching
  d) Load pulling test

o Small-signal model of a bipolar transistor

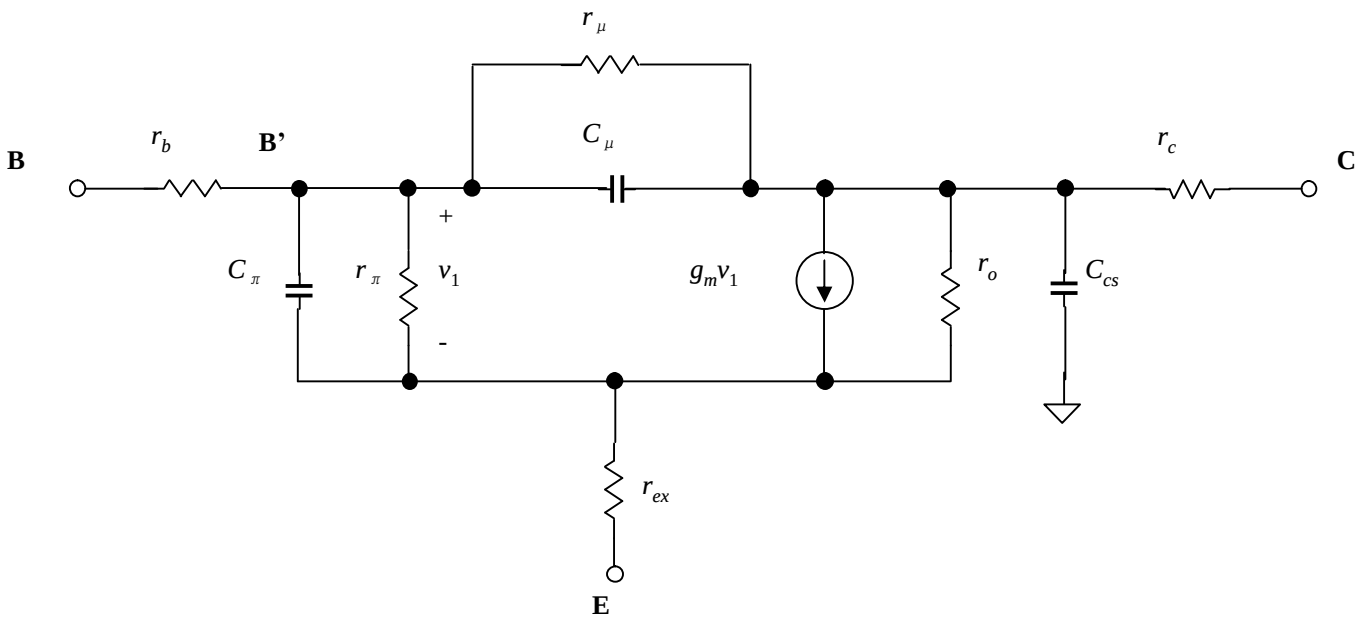


Figure 6.2 Small-signal equivalent circuit model of a bipolar transistor

$$I_c = I_s\left(1+\frac{V_{ce}}{V_A}\right)\exp\left(\frac{V_{be}}{V_T}\right) = I_s\left(1+\frac{V_{ce}}{V_A}\right)\exp\left(\frac{qV_{be}}{kT}\right)$$

$$g_m = \frac{\partial I_c}{\partial V_{be}} = I_s\left(1+\frac{V_{ce}}{V_A}\right)\frac{q}{kT}\exp\left(\frac{qV_{be}}{kT}\right) = \frac{qI_c}{kT}$$

$$C_p = C_b + C_{je} \qquad r_p = \frac{b_o}{g_m}$$

$$C_b = t_F g_m \qquad r_o = \frac{V_A}{I_c}$$

$$C_{je} = \frac{C_{jeo}}{\sqrt[3]{1-\frac{V_D}{y_o}}} \qquad r_m = (1 \to 10) b_o r_o$$

$$C_m = \frac{C_{mo}}{\left(1-\frac{V}{y_o}\right)^n}$$

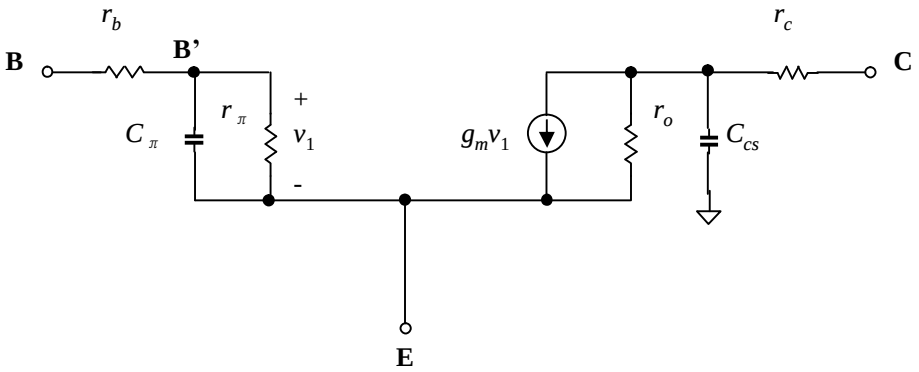


Figure 6.3 Small-signal equivalent circuit model of a bipolar transistor in the high frequency.

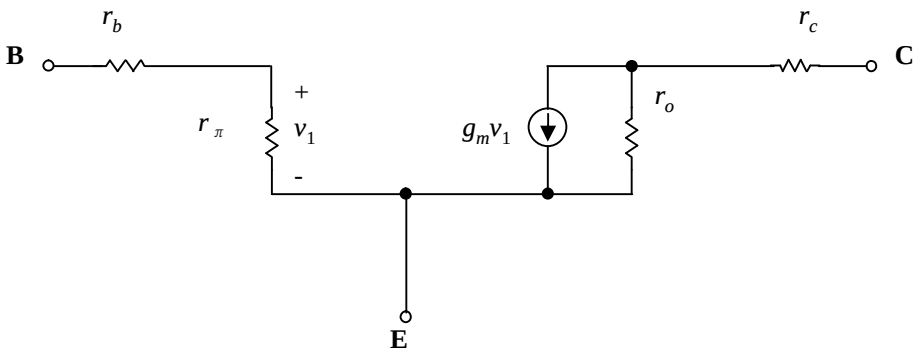


Figure 6.4 Small-signal equivalent circuit model of a bipolar transistor in the low frequency

* **Impedance of a CE (common emitter) device**

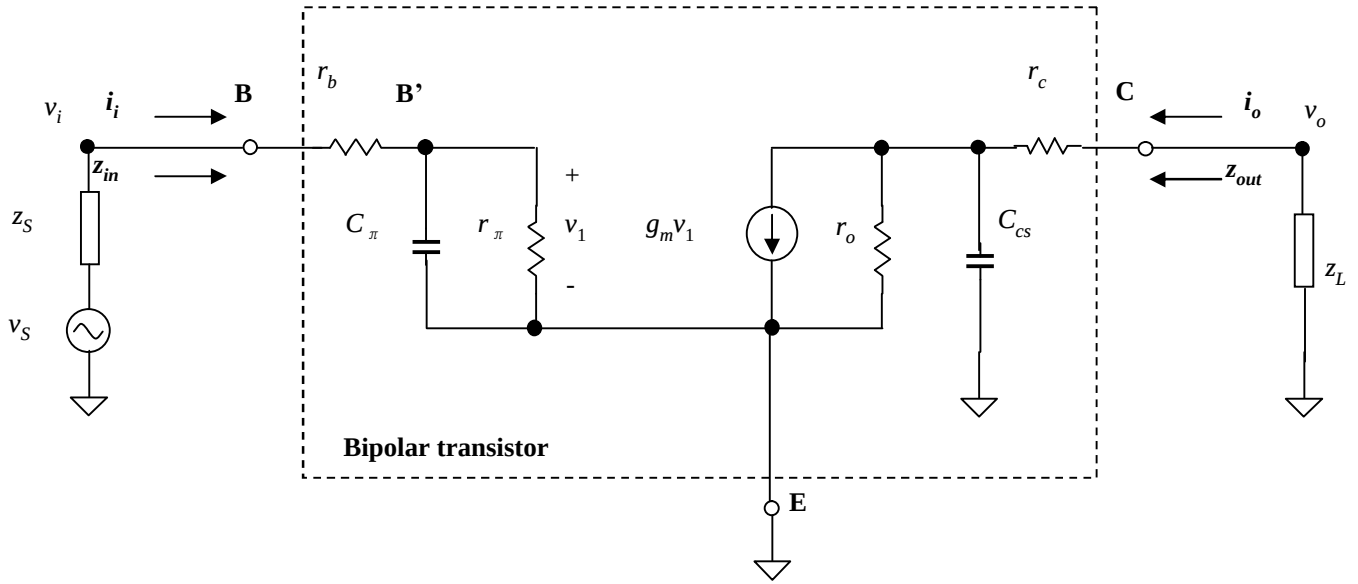


Figure 6.5 Small-signal equivalent circuit model of a CE (common emitter) device

$$z_{in} = r_b + \frac{1}{jC_p w} // r_p$$

$$Q = \frac{1}{r_S C_S w} = r_p C_p w \qquad r_S = \frac{r_p}{(Q^2+1)} = \frac{r_p}{(r_p C_p w)^2 + 1}$$

$$C_S = C_p \frac{Q^2+1}{Q^2} = C_p \frac{(r_p C_p w)^2 + 1}{(r_p C_p w)^2}$$

$$z_{in} = \left[r_b + \frac{r_p}{(r_p C_p w)^2 + 1} \right] - j \frac{(r_p C_p w)^2}{C_p w[(r_p C_p w)^2 + 1]}$$

$$z_{out} = r_c + r_o // \frac{1}{jC_{cs} w}$$

$$z_{out} = \left[r_c + \frac{r_o}{(r_o C_{cs} w)^2 + 1} \right] - j \frac{(r_o C_{cs} w)^2}{C_{cs} w[(r_o C_{cs} w)^2 + 1]}$$

In the low-and mid-frequency, the capacitors, C_π and C_{CS}, are negligible, thus

$$z_{in} = r_b + r_p$$

$$z_{out} = r_c + r_o$$

* **Impedance of a CB (common base) device**

Approximations : $r_b << r_p$ $\qquad$ $r_p << r_o$

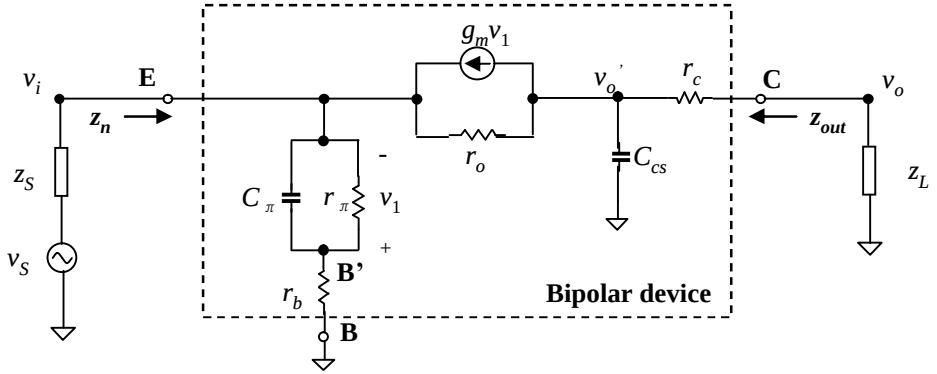


Figure 6.6 Small-signal equivalent circuit model of a CB (common base) device

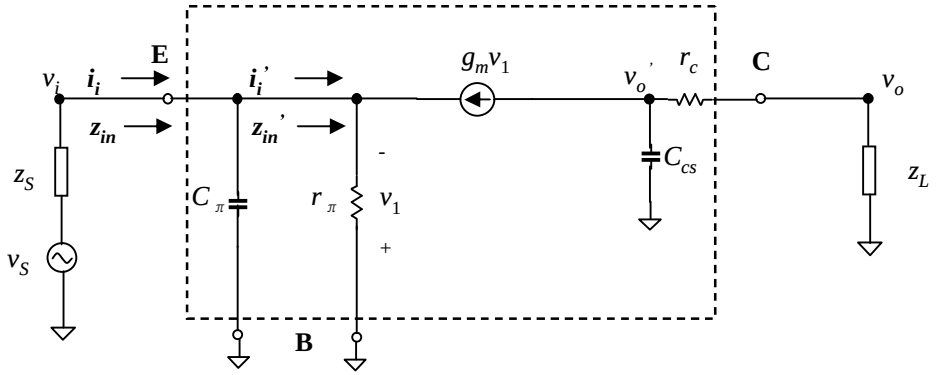


Figure 6.7 Small-signal equivalent circuit model of a CB (common base) device for input impedance discussion

$$v_i = -v_1$$

$$z_{in}' = \frac{v_i}{i_i'} = \frac{v_i}{\frac{v_i}{r_p} - g_m v_1} = \frac{v_i}{\frac{v_i}{r_p} + g_m v_i} = \frac{r_p}{1 + g_m r_p} \approx \frac{1}{g_m}$$

$$z_{in} = \frac{1}{jC_p w} // z_{in}' = \frac{r_p}{1 + r_p (g_m + jC_p w)} \approx \frac{1}{g_m + jC_p w}$$

However for higeraccuracy when r_o is taken into account,
the input impedance is dependent of the load, z_L. It would be modified to

$$z_{in} = \frac{r_p}{1 + r_p (g_m + jC_p w)} \left(1 + \frac{r_c + z_L}{r_o} \right)$$

At low-and mid-frequency,

$$z_{in} = \frac{r_p}{1 + r_p g_m} \left(1 + \frac{r_c + z_L}{r_o} \right)$$

For higher accuracy, the resistor r_b is taken into account,

$$z_{in} = \frac{r_p + r_b}{1 + (r_p + r_b) g_m} \left(1 + \frac{r_c + z_L}{r_o} \right)$$

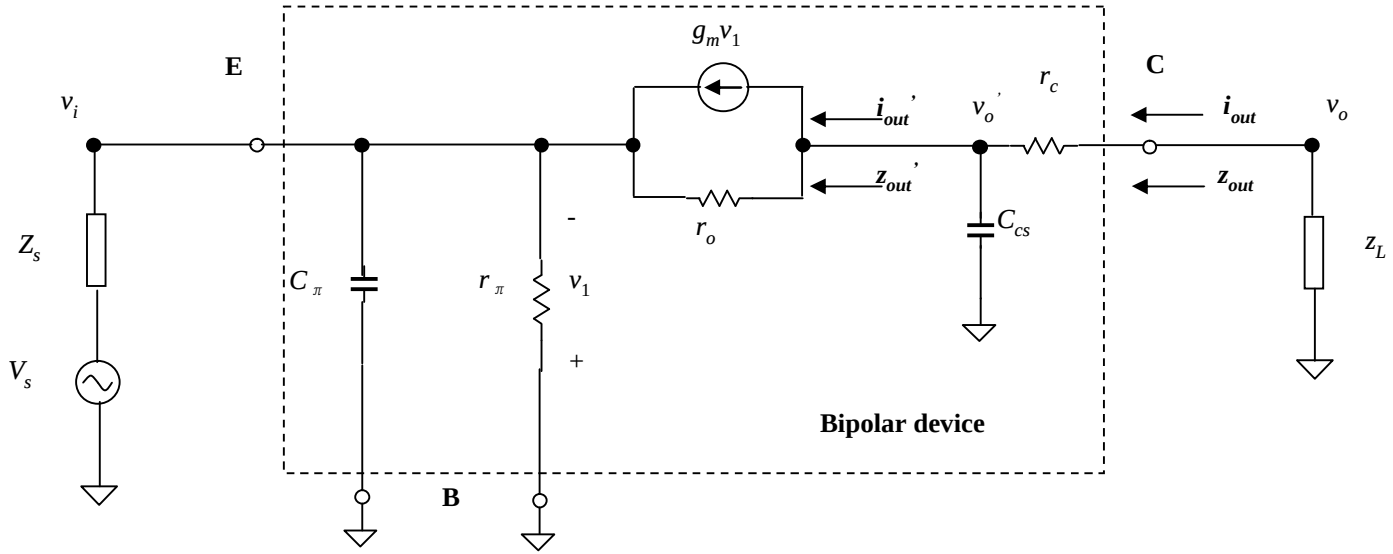


Figure 6.8 Small-signal equivalent circuit model of a CB (common base) device for output impedance discussion

$$i_{out}' = g_m v_1 + \frac{v_o' - v_i}{r_o} = -g_m v_i + \frac{v_o' - v_i}{r_o}$$

$$i_{out} = i_{out}' + \frac{v_o'}{\frac{1}{jC_{CS}w}} = \frac{v_o'}{r_o + R(1+g_m r_o)} + v_o' jC_{CS}w = \left[\frac{1}{r_o + R(1+g_m r_o)} + jC_{CS}w\right] v_o'$$

$$-\frac{v_i}{z_s // r_p // C_p} + \frac{v_o' - v_i}{r_o} + g_m(-v_i) = 0$$

$$v_i = \frac{1}{r_o(\frac{1}{R} + \frac{1}{r_o} + g_m)} v_o'$$

$$v_o = i_{out} r_c + v_o'$$

$$z_{out}' = \frac{v_o'}{i_{out}'} = r_o + R(1+g_m r_o)$$

$$z_{out} = \frac{v_o}{i_{out}} = r_c + r_o + R(1+g_m r_o)$$

$$z_{out} = \frac{v_o}{i_{out}} = r_c + \frac{1}{\frac{1}{r_o + R(1+g_m r_o)} + jC_{CS}w}$$

$$R = z_s // r_p // C_p = \frac{z_s r_p \frac{1}{jC_p w}}{z_s r_p + r_p \frac{1}{jC_p w} + z_s \frac{1}{jC_p w}} \qquad R = \frac{z_s r_p}{z_s + r_p + jC_p w z_s r_p} \qquad R = \frac{z_s r_p}{z_s + r_p}$$

* **Impedance of a CC (common collector) device**

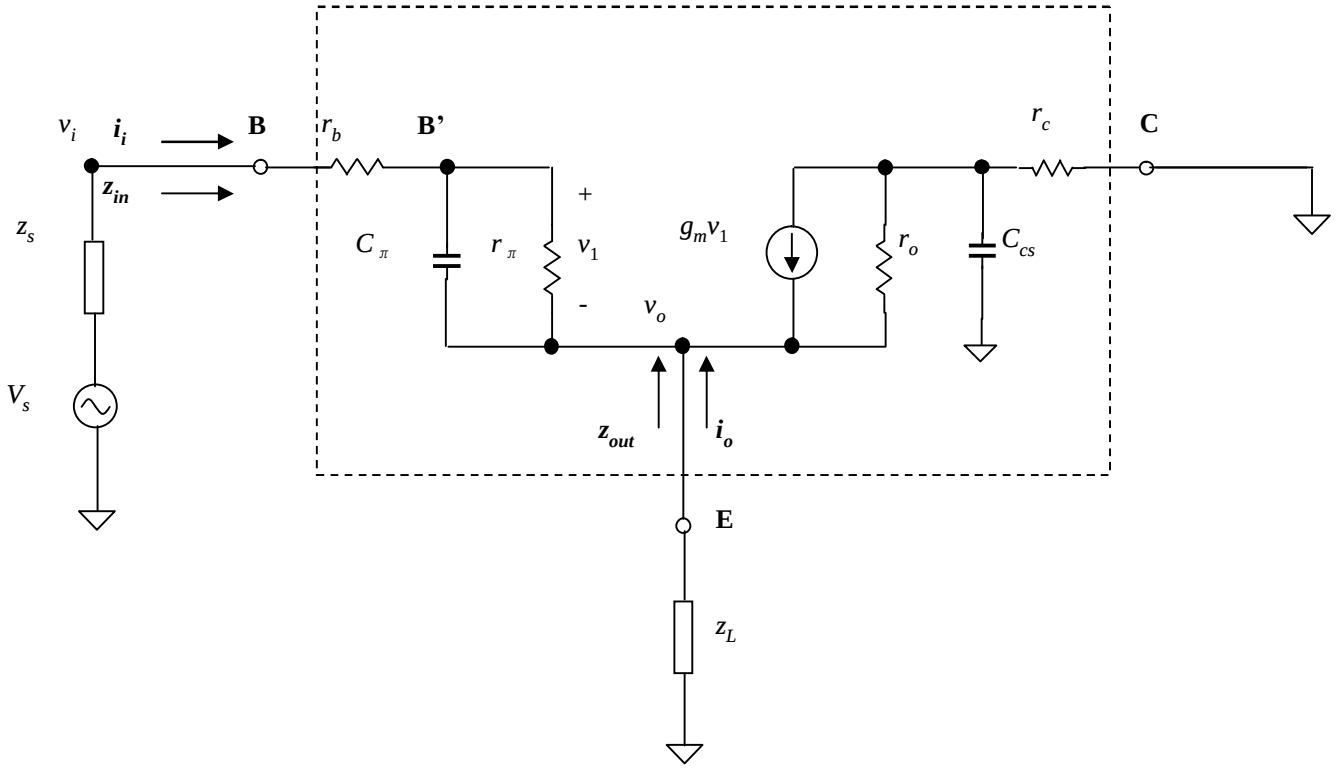


Figure 6.9 Small-signal equivalent circuit model of a CC (common collector) device

$$v_o = (i_i + g_m v_1)[z_L // (r_o + r_c // C_{cs})]$$

$$v_o = i_i[1 + g_m(r_p // C_p)][z_L // (r_o + r_c // C_{cs})]$$

$$v_i = i_i(r_b + r_p // C_p) + i_i[1 + g_m(r_p // C_p)][z_L // (r_o + r_c // C_{cs})]$$

$$z_{in} = \frac{v_i}{i_i} = (r_b + r_p // C_p) + [1 + g_m(r_p // C_p)][z_L // (r_o + r_c // C_{cs})]$$

$$r_p // C_p = \frac{1}{1 + jC_p w r_p} r_p$$

$$r_b + r_p // C_p = \frac{r_b + r_p + jC_p w r_b r_p}{1 + jC_p w r_p}$$

$$r_o + r_c // C_{cs} = \frac{r_o + r_c + jC_{cs} w r_o r_c}{1 + jC_{cs} w r_c}$$

$$z_L // (r_o + r_c // C_{cs}) = \frac{r_o + r_c + jC_{cs} w r_o r_c}{z_L + r_o + r_c + jC_{cs} w r_c (r_o + Z_L)} z_L$$

$$z_{in} = \frac{r_p + r_b(1 + jC_p w r_p) + (1 + b + jC_p w r_p)\dfrac{r_o + r_c + jC_{cs} w r_o r_c}{z_L + r_o + r_c + jC_{cs} w r_c (r_o + Z_L)} z_L}{1 + jC_p w r_p}$$

$$i_o = \frac{v_o}{r_o + (r_c // C_{cs})} + g_m \frac{(r_p // C_p) v_o}{z_s + r_b + (r_p // C_p)} + \frac{v_o}{z_s + r_b + (r_p // C_p)}$$

$$i_o = \frac{1 + jC_{cs} w r_c}{r_c + r_o (1 + jC_{cs} w r_c)} v_o + \frac{1 + b + jC_p w r_p}{r_p + (Z_s + r_b)(1 + jC_p w r_p)} v_o$$

$$\frac{1}{z_{out}} = \frac{i_o}{v_o} = \frac{1 + jC_{cs} w r_c}{r_c + r_o (1 + jC_{cs} w r_c)} + \frac{1 + b + jC_p w r_p}{r_p + (z_s + r_b)(1 + jC_p w r_p)}$$

$$z_{out} = \frac{[r_c + r_o (1 + jC_{cs} w r_c)][r_p + (z_s + r_b)(1 + jC_p w r_p)]}{(1 + jC_{cs} w r_c)[r_p + (z_s + r_b)(1 + jC_p w r_p)] + (1 + b + jC_p w r_p)[r_c + r_o (1 + jC_{cs} w r_c)]}$$

At the low-and mid-frequency,

$$z_{in} \approx r_p + r_b + (1 + b) \frac{r_o + r_c}{z_L + r_o + r_c} z_L$$

$$z_{out} \approx \frac{(r_c + r_o)(z_s + r_b + r_p)}{(1 + b)(r_c + r_o) + (z_s + r_b + r_p)}$$

$r_o >> z_L$ $\qquad z_{in} \approx r_p + r_b + (1 + b) z_L$

$r_p >> z_s$ $\qquad z_{out} \approx \dfrac{1}{1 + b + \dfrac{r_p}{r_c + r_o}} r_p$

$r_o >> r_p$ $\qquad z_{out} \approx \dfrac{1}{g_m}$

* **Comparison between CE, CB, and CC devise**

Table 6.2 Input and output impedances of a bipolar amplifierwith CE,CB, and CC configuration in low frequency.
$Z_{L,A}$ = Actual load impedance

Input impedance	*Output impedance*	Z_L _____.
CE (Common emitter)		
$z_{in} = r_p + r_b$	$z_{out} = r_o + r_c$	
CB (Common base)		
$z_{in} \approx \frac{r_p + r_b}{1 + (r_p + r_b) g_m} \left(1 + \frac{r_c + z_L}{r_o}\right)$	$z_{out} \approx r_o + r_c + \frac{z_s r_p}{z_s + r_p}(1 + g_m r_o)$	$z_L = R_C // z_{L,A}$
CC (Common collector, or Emitter follower)		
$z_{in} \approx r_p + r_b + (1+b)\frac{r_o + r_c}{z_L + r_o + r_c} z_L$	$z_{out} \approx \frac{(r_o + r_c)(z_s + r_b + r_p)}{(1+b)(r_o + r_c) + (z_s + r_b + r_p)}$	$z_L = R_E // z_{L,A}$

o Small-signal model of a MOSFET transistor

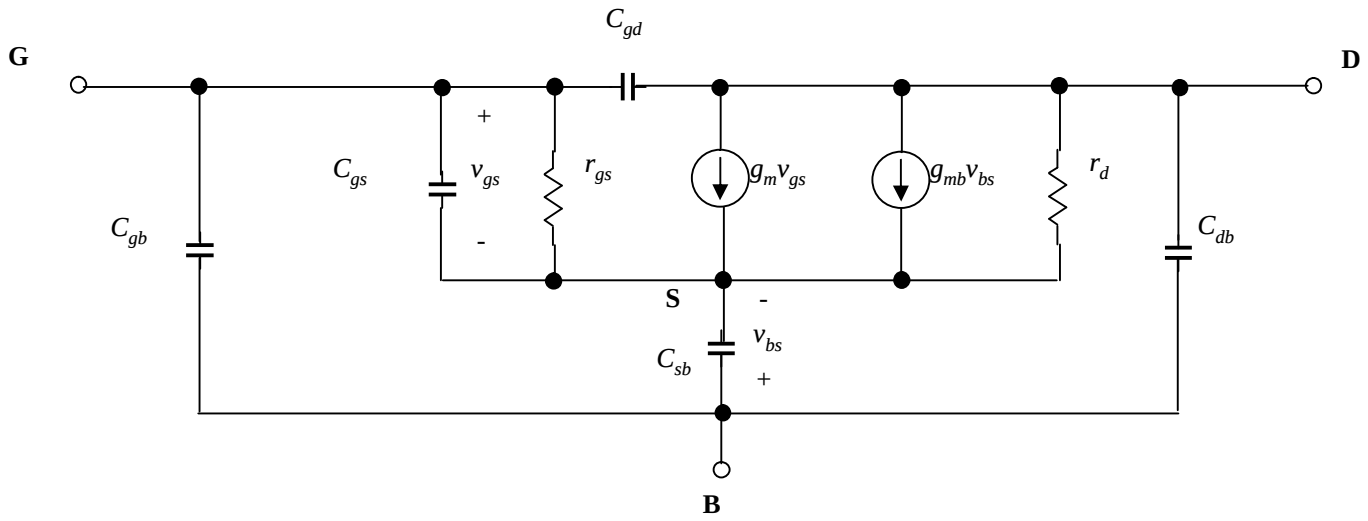


Figure 6.10 Small-signal equivalent circuit model of a MOSFET transistor

$$I_d = \frac{k'}{2}\frac{W}{L}(V_{gs} - V_t)^2(1 + lV_{ds})$$

$$g_m = \frac{\partial I_d}{\partial V_{gs}} = k'\frac{W}{L}(V_{gs} - V_t)(1 + lV_{ds})$$

$lV_{ds} << 1$

$$I_d = \frac{k'}{2}\frac{W}{L}(V_{gs} - V_t)^2$$

$$g_m \approx k'\frac{W}{L}(V_{gs} - V_t) = \sqrt{2k'\frac{W}{L}I_d}$$

$$g_{mb} = c = \frac{C_{js}}{C_{ox}}$$

$$r_o = \frac{1}{lI_d} = \frac{V_A}{I_d}$$

$$C_{gs} = \frac{2}{3}WLC_{ox}$$

$$f_t = \frac{1}{2p}\frac{g_m}{C_{gs} + C_{gd} + C_{gb}}$$

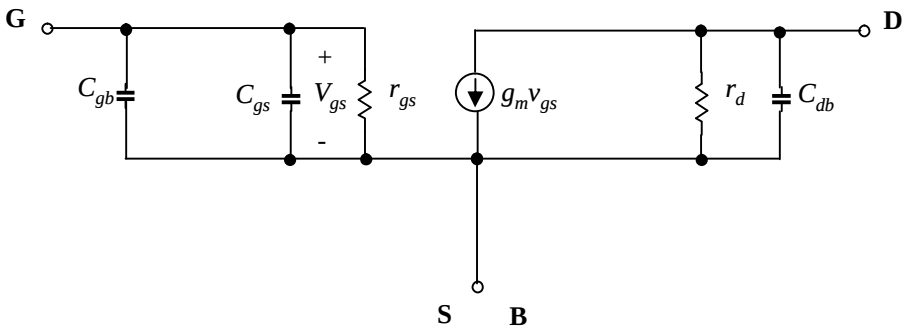


Figure 6.11 Small-signal equivalent circuit model of a MOSFET transistor in the high frequency (The source, S, is connected to the body, B.)

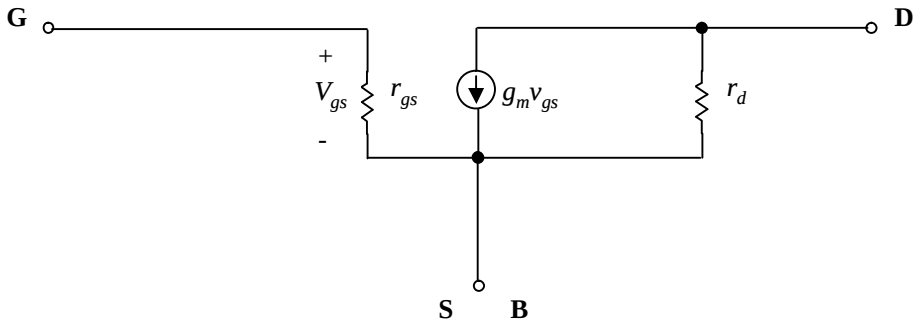


Figure 6.12 Small-signal equivalent circuit model of a MOSFET transistor in the low frequency (The source, S, is connected to the body, B.)

Translation

The similarity between bipolar and MOSFET model provides a short-cut to translate all of input and output impedance formula from the bipolar to MOSFET transistor, as longas we do the following replacements:

C_μ **à** C_{gd},
C_{cs} **à** C_{db},
C_π **à** $(C_{gs}+C_{gb})$,
C_{sb} **à** infinitive

r_μ **à** 0,
r_{ex} **à** 0,
r_b **à** 0,

r_c **à** 0,
r_π **à** r_{gs},
r_o **à** r_d,
β_o **à** $g_m r_{gs}$.

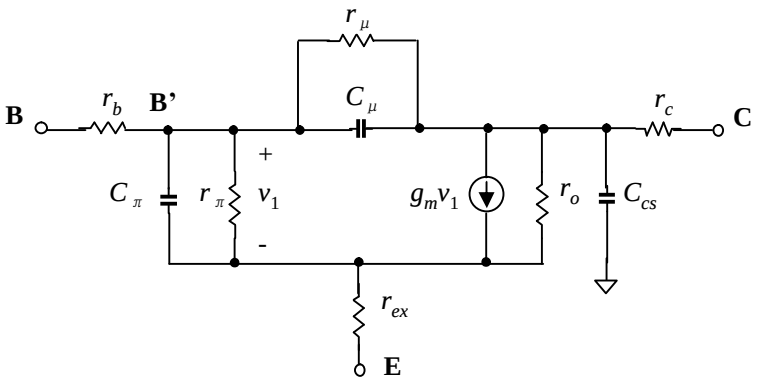


Figure 6.13 Small-signal equivalent circuit model of a bipolar transistor

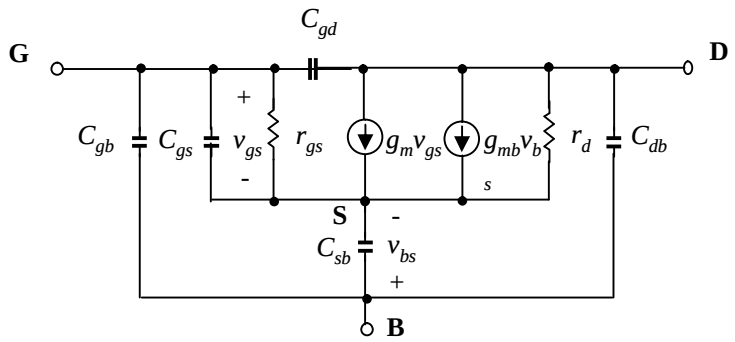


Figure 6.14 Small-signal equivalent circuit model of a MOSFET transistor

* **Impedance of a CS (common source) device**

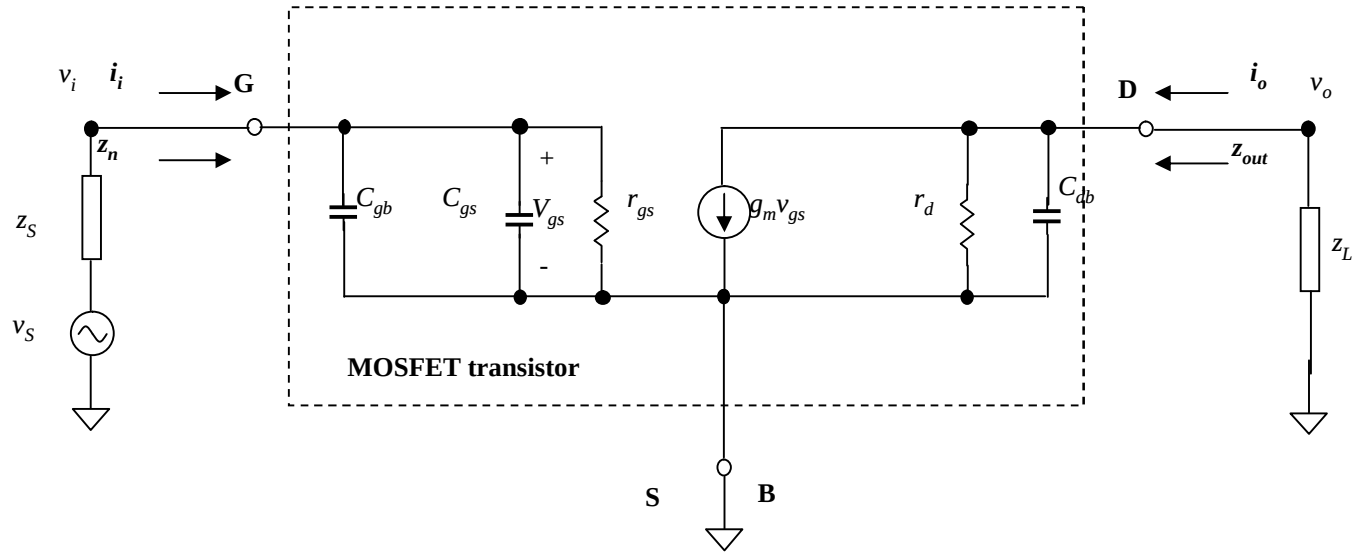


Figure 6.15 Small-signal equivalent circuit model of a CS (common source) device

$$z_{in} = \frac{r_{gs}}{[r_{gs}(C_{gs}+C_{gb})w]^2+1} - j\frac{[r_{gs}(C_{gs}+C_{gb})w]^2}{(C_{gs}+C_{gb})w\{[r_{gs}(C_{gs}+C_{gb})w]^2+1\}}$$

$$z_{out} = \frac{r_d}{(r_d C_{db} w)^2+1} - j\frac{(r_d C_{db} w)^2}{C_{db} w[(r_d C_{db} w)^2+1]}$$

At the low-and mid-frequency,

$$z_{in} = r_{gs}$$

$$z_{out} = r_d$$

* **Impedance of a CG (common gate) device**

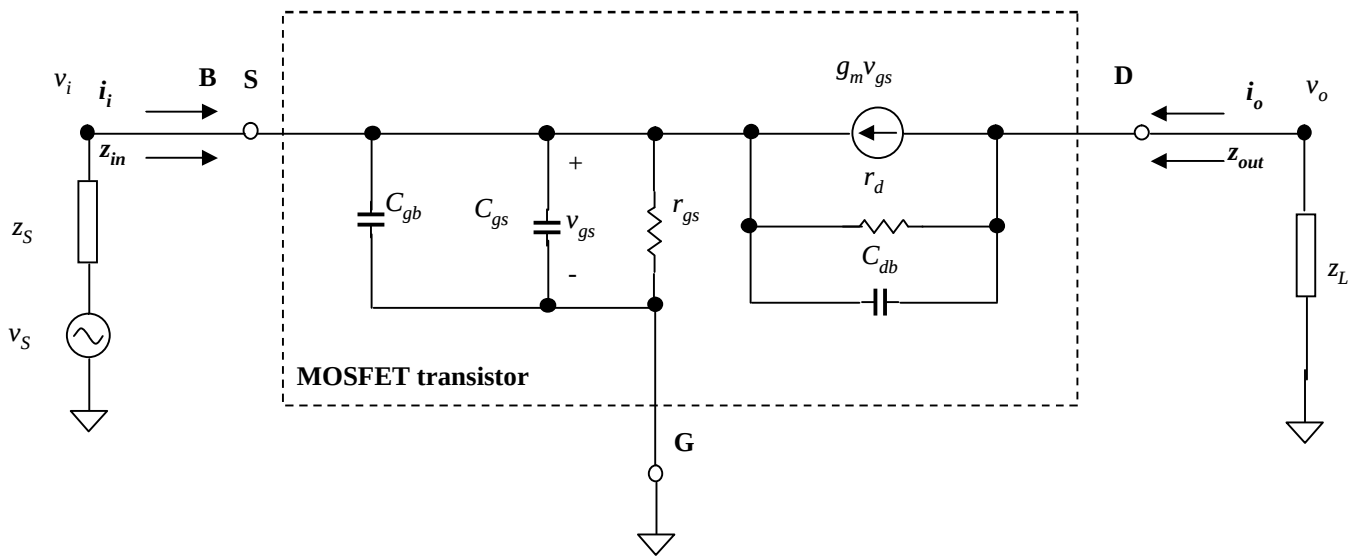


Figure 6.16 Small-signal equivalent circuit model of a CG (common gate) device

$$z_{in} = \frac{r_{gs}}{1 + r_{gs}[g_m + j(C_{gs} + C_{gb}w)]}\left(1 + \frac{z_L}{r_d}\right) \qquad z_{out} = \frac{1}{\dfrac{1}{r_d + \dfrac{z_s r_{gs}}{z_s + r_{gs} + j(C_{gs} + C_{gb})w}(1 + g_m r_d)} + jC_{db}w}$$

At the low-and mid-frequency,

$$z_{in} \approx \frac{r_{gs}}{1 + r_{gs} g_m}\left(1 + \frac{z_L}{r_d}\right) \qquad z_{out} \approx r_d + \frac{z_s r_{gs}}{z_s + r_{gs}}(1 + g_m r_d)$$

* **Impedance of a CD (common drain) device**

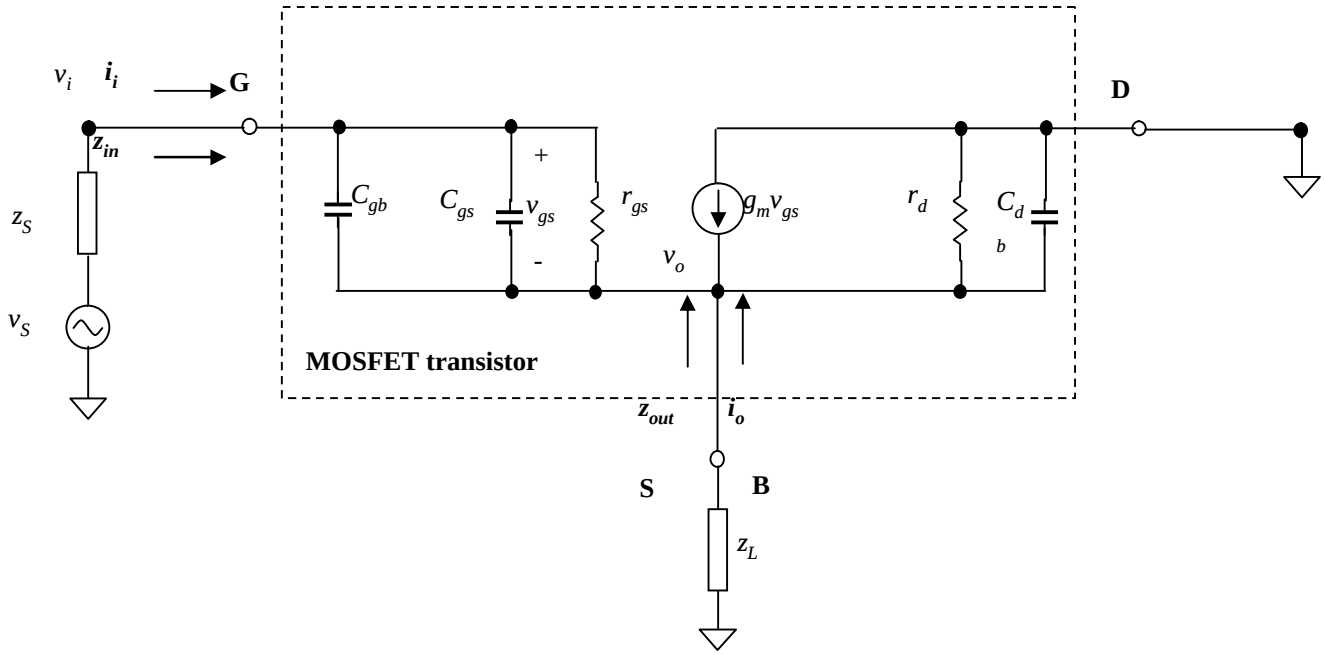


Figure 6.17 Small-signal equivalent circuit model of a CD (common drain) device

$$z_{in} = \frac{r_{gs} + [1 + g_m r_{gs} + j(C_{gs} + C_{gb})w r_{gs}]\dfrac{r_d}{z_L + r_d} z_L}{1 + j(C_{gs} + C_{gb})w r_{gs}}$$

$$z_{out} = \frac{r_d\{r_{gs} + z_s[1 + j(C_{gs} + C_{gb})w r_{gs}]\}}{r_{gs} + z_s[1 + j(C_{gs} + C_{gb})w r_{gs}] + r_d[1 + g_m r_{gs} + j(C_{gs} + C_{gb})w r_{gs}]}$$

At the low-and mid-frequency,

$$z_{in} \approx r_{gs} + (1 + g_m r_{gs})\frac{r_d}{z_L + r_d} z_L \qquad z_{out} \approx \frac{r_d(z_s + r_{gs})}{(1 + g_m r_{gs})r_d + (z_s + r_{gs})}$$

.

* **Comparison between CS, CG, and CD devise**

Table 5.3 Input and output impedances of MOSFET transistor with CS,CG, and CDconfiguration in low and mid-frequency.

Input impedance	*Output impedance*	Z_L _____ .
CS (Common source)		
$z_{in} = r_{gs}$	$z_{out} = r_d$	
CG (Common gate)		
$z_{in} \approx \frac{r_{gs}}{1 + r_{gs} g_m} \left(1 + \frac{z_L}{r_d} \right)$	$z_{out} \approx r_d + \frac{z_s r_{gs}}{z_s + r_{gs}} (1 + g_m r_d)$	$z_L = R_d // z_{L,A}$
CD (Common drain or source follower)		
$z_{in} \approx r_{gs} + \left(1 + g_m r_{gs}\right) \frac{r_d}{z_L + r_d} z_L$	$z_{out} \approx \frac{r_d \left(z_s + r_{gs} \right)}{\left(1 + g_m r_{gs}\right) r_d + \left(z_s + r_{gs} \right)}$	$z_L = R_S // z_{L,A}$

2. Differential pair

o DC transfer characteristic

* Bipolar differential pair

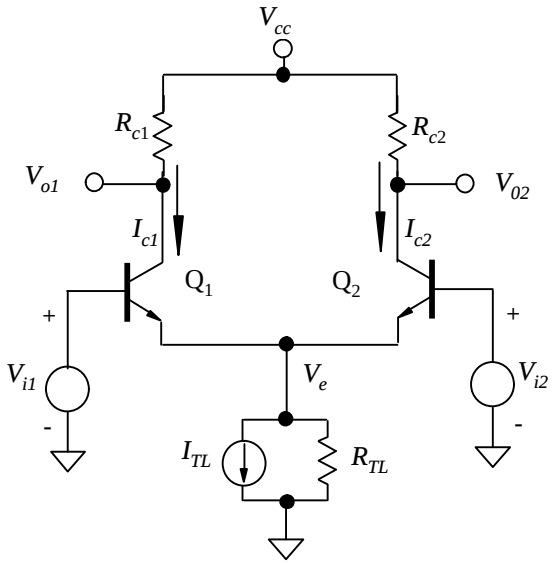


Figure 6.18 A differential pair with bipolar devices

In the loop of V_{i1} à emitter of Q_1 à V_e à emitter of Q_2 à V_{i2},

$$V_{i1} - V_{be1} + V_{be2} - V_{i2} = 0$$

$$V_{be1} = V_T \ln \frac{I_{c1}}{I_{S1}\left(1 + \frac{V_{ce1}}{V_{A1}}\right)} \qquad V_{be2} = V_T \ln \frac{I_{c2}}{I_{S2}\left(1 + \frac{V_{ce2}}{V_{A2}}\right)}$$

Assuming that the transistors are identical, that is

$$I_{s1} = I_{s2} = I_s$$

$$V_{ce1} = V_{ce2} = V_{ce}$$

$$V_{A1} = V_{A2} = V_A$$

$$a_{F1} = a_{F2} = a_F$$

$$\frac{I_{c1}}{I_{c2}} = \exp\left(\frac{V_{be1} - V_{be2}}{V_T}\right) = \exp\left(\frac{V_{i1} - V_{i2}}{V_T}\right) = \exp\left(\frac{V_{id}}{V_T}\right)$$

$$V_{id} = V_{i1} - V_{i2}$$

$$-\left(I_{e1} + I_{e2}\right) = I_{TL} = \frac{I_{c1} + I_{c2}}{a_F}$$

$$I_{c1} = \frac{a_F I_{TL}}{1 + \exp\left(-\frac{V_{id}}{V_T}\right)} \qquad I_{c2} = \frac{a_F I_{TL}}{1 + \exp\left(\frac{V_{id}}{V_T}\right)}$$

$$V_{o1} = V_{cc} - I_{c1} R_c \qquad V_{o2} = V_{cc} - I_{c2} R_c$$

$$R_{c1} = R_{c2} = R_c$$

$$V_{od} = V_{o1} - V_{o2} = a_F I_{TL} R_c \tanh\left(\frac{-V_{id}}{2V_T}\right)$$

***CMOS differential pair**

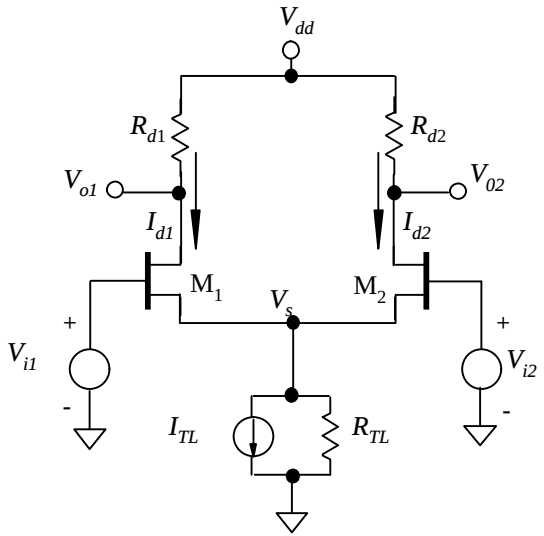


Figure 6.19 A differential pair with CMOS device

In the loop of V_{i1} à source of M_1 à V_s à source of M_2 à V_{i2},

$$V_{i1} - V_{gs1} + V_{gs2} - V_{i2} = 0$$

$$V_{gs1} - V_t = \sqrt{\frac{2I_{d1}}{k'\frac{W_1}{L_1}(1 + lV_{ds1})}} \qquad V_{gs2} - V_t = \sqrt{\frac{2I_{d2}}{k'\frac{W_2}{L_2}(1 + lV_{ds2})}}$$

Assuming that the transistors are identical, that is

$$W_1 = W_2 = W \qquad L_1 = L_2 = L$$

$$V_{ds1} = V_{ds2} = V_{ds}$$

$$V_{id} = V_{i1} - V_{i2} = V_{gs1} - V_{gs2} = \frac{\sqrt{I_{d1}} - \sqrt{I_{d2}}}{\sqrt{\frac{k'}{2}\frac{W}{L}(1 + lV_{ds})}}$$

$$I_{d1} + I_{d2} = I_{TL}$$

$$I_{d1} = \frac{I_{TL}}{2} + \frac{k'}{4}\frac{W}{L}(1 + lV_{ds})V_{id} = \sqrt{\frac{4I_{TL}}{\frac{k'}{2}\frac{W}{L}(1 + lV_{ds})} - V_{id}^2} \qquad I_{d2} = \frac{I_{TL}}{2} - \frac{k'}{4}\frac{W}{L}(1 + lV_{ds})V_{id} = \sqrt{\frac{4I_{TL}}{\frac{k'}{2}\frac{W}{L}(1 + lV_{ds})} - V_{id}^2}$$

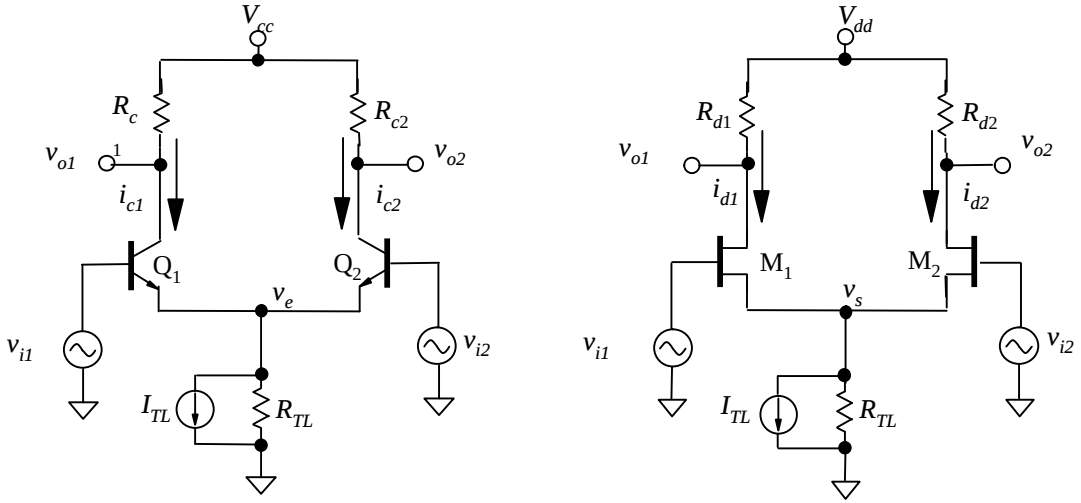
$$\Delta I_d = I_{d1} - I_{d2} = \frac{k'}{2}\frac{W}{L}(1 + lV_{ds})V_{id}\sqrt{\frac{4I_{TL}}{\frac{k'}{2}\frac{W}{L}(1 + lV_{ds})} - V_{id}^2}$$

$$V_{od} = V_{o1} - V_{o2} = (V_{dd} - I_{d1}R_d) - (V_{dd} - I_{d2}R_d) = -\Delta I_d R_d$$

$$V_{od} = -R_d \frac{k'}{2}\frac{W}{L}(1 + lV_{ds})V_{id}\sqrt{\frac{4I_{TL}}{\frac{k'}{2}\frac{W}{L}(1 + lV_{ds})} - V_{id}^2}$$

o Small signal characteristic

Important reference : Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, and Robert G. Meyer,"Analysis and Design of Analog Integrated Circuits," (Book), Fourth Edition, John Wiley & Sons, Inc., 2001.



(a) A differential pair with bipolar devices (b)A differential pair with MOSFETdevices

Figure 6.20 Differential pair

$$v_{o1} = A_{11}v_{i1} + A_{12}v_{i2}$$

$$v_{o2} = A_{21}v_{i1} + A_{22}v_{i2}$$

$$v_{ic} = \frac{v_{i1} + v_{i2}}{2}$$

$$v_{id} = v_{i1} - v_{i2}$$

$$v_{od} = v_{o1} - v_{o2}$$

$$v_{oc} = \frac{v_{o1} + v_{o2}}{2}$$

$$A_{dm} = \frac{A_{11} - A_{12} - A_{21} + A_{22}}{2}$$

$$A_{dm-cm} = \frac{A_{11} - A_{12} + A_{21} - A_{22}}{4}$$

$$A_{cm-dm} = A_{11} + A_{12} - A_{21} - A_{22}$$

$$A_{cm} = \frac{A_{11} + A_{12} + A_{21} + A_{22}}{2}$$

$$v_{od} = A_{dm}v_{id} + A_{cm-dm}v_{ic}$$

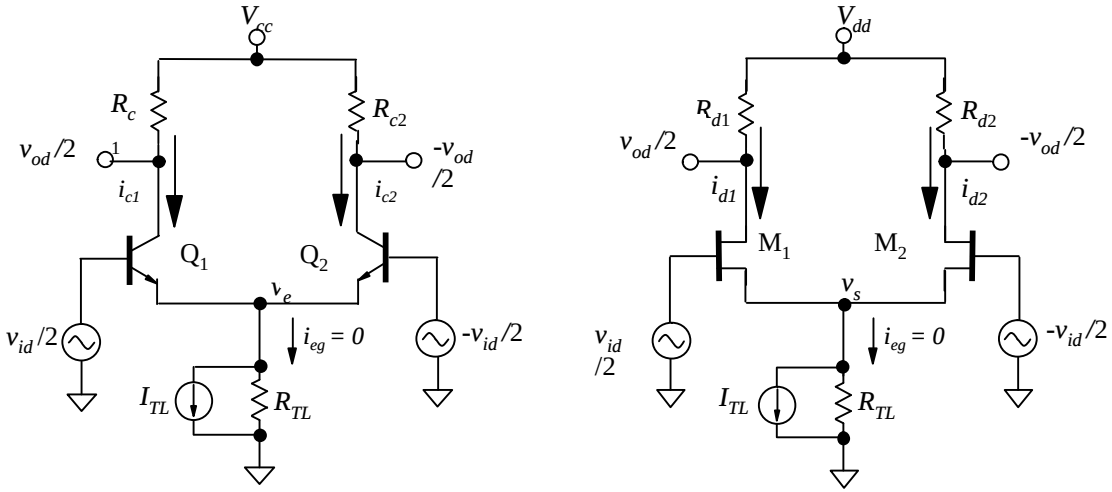
$$v_{oc} = A_{dm-cm}v_{id} + A_{cm}v_{ic}$$

$$v_{i1} = v_{ic} + \frac{v_{id}}{2}$$

$$v_{i2} = v_{ic} - \frac{v_{id}}{2}$$

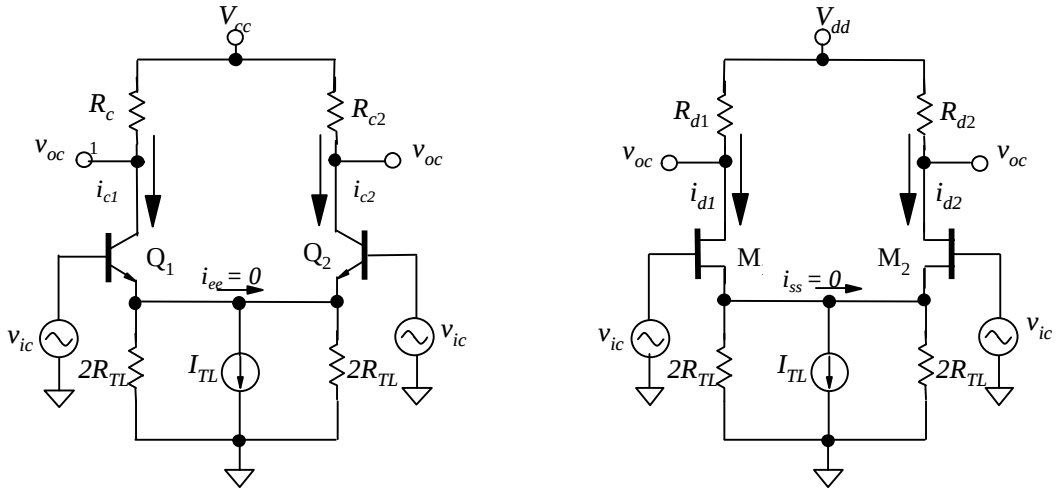
$$v_{o1} = v_{oc} + \frac{v_{od}}{2}$$

$$v_{o2} = v_{oc} - \frac{v_{od}}{2}$$



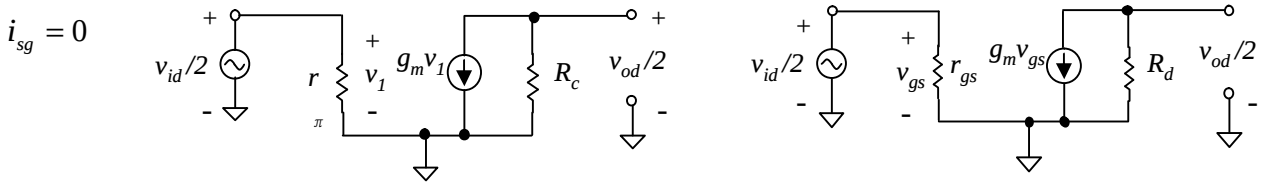
(a) Bipolar devices (b)MOSFETdevices

Figure 6.21 Differential mode portion of a differential pair



(a) Bipolar devices (b)MOSFETdevices

Figure 6.22 Commonmode portion of a differential pair



(a) Bipolar device

Approximation:

$r_b \to 0$ $\quad C_\pi \to 0$

$r_o \to \infty$ $\quad C_{cs} \to 0$

$r_c \to 0$

(b) MOSFET transistor

Approximation:

$r_d \to \infty$ $\quad C_{gd} \to 0$

$C_{db} \to 0$ $\quad C_{gb} \to 0$

$C_{sb} \to 0$ $\quad C_{gs} \to 0$

Figure 6.23 Equivalent of differential mode half circuit

$$\frac{v_{od}}{2} = -g_m v_1 R_c = -g_m \frac{v_{id}}{2} R_c$$

$$\frac{v_{od}}{2} = -g_m v_{gs} R_d = -g_m \frac{v_{id}}{2} R_d$$

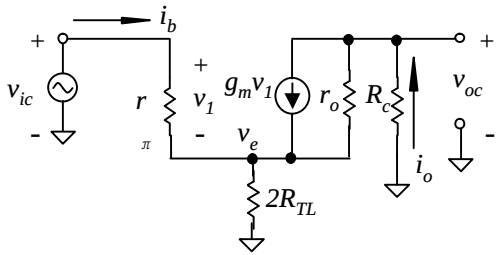
$$R_c = R_{c1} = R_{c2}$$

$$R_d = R_{d1} = R_{d2}$$

$$\frac{v_{od}}{2} = -g_m \frac{v_{id}}{2} R$$

$$A_{dm} = \frac{v_{od}}{v_{id}} = -g_m R$$

$i_{ee} = i_{ss} = 0$

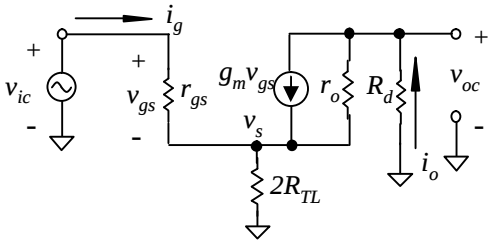


(a) Bipolar device

Approximation:

$r_b \to 0$ $\quad C_\pi \to 0$

$r_c \to 0$ $\quad C_{cs} \to 0$



(b) MOSFET

Approximation:

$C_{db} \to 0$ $\quad C_{gd} \to 0$

$C_{sb} \to 0$ $\quad C_{gb} \to 0$

$C_{gs} \to 0$

Figure 6.24 Equivalent of common mode half circuit

$$G_m = \frac{i_o}{v_{ic}} = g_m \frac{g_m}{1 + 2g_m R_{TL}(g_m r_p + 1)}$$

$$G_m = \frac{i_o}{v_{ic}} = \frac{g_m}{1 + 2g_m R_{TL}(g_m r_{gs} + 1)}$$

$$G_m = \frac{i_o}{v_{ic}} = \frac{g_m}{1 + 2g_m R_{TL}(g_m r_{p\,gs} + 1)}$$

$r_o >> R_{TL}$

$$v_{oc} = -i_o R = -G_m R v_{ic}$$

$$A_{cm} = \frac{v_{oc}}{v_{ic}} = -G_m R = -\frac{g_m R}{1 + 2g_m R_{TL}(g_m r_{pgs} + 1)}$$

* **CMRR (Common Mode Rejection Ratio)**

$$CMRR = \frac{A_{dm}}{A_{cm}} = 1 + 2g_m R_{TL}\left(1 + \frac{1}{g_m r_{pgs}}\right)$$

*** CMRR caused by a single-ended device**

$$\boldsymbol{v_{i2} = v_{o2} = 0}$$

$$v_{id} = v_{i1}$$
$$v_{ic} = v_{i1}/2$$

$$v_{od} = v_{o1}$$
$$v_{oc} = v_{o1}/2$$

and

$$v_{o1} = A_{11} v_{i1}$$
$$0 = A_{21} v_{i1}$$

or,

$$v_{od} = A_{dm} \quad v_{id} + A_{cm\text{-}dm} v_{ic}/2$$
$$v_{oc} = A_{dm\text{-}cm} v_{id} + A_{cm} \quad v_{ic}/2$$

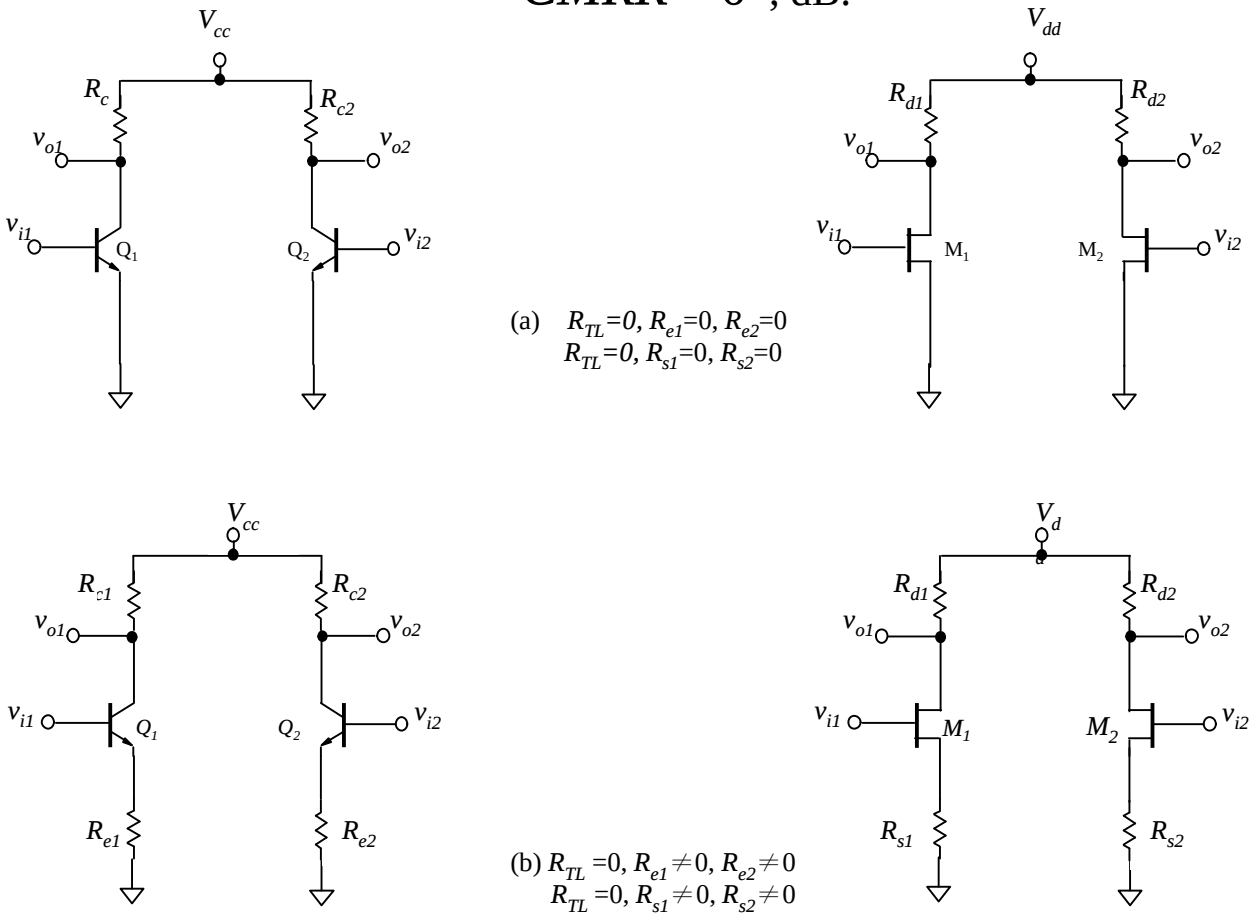
$$\boldsymbol{\text{CMRR} = A_{dm} / A_{cm} = 1}$$

* **A pseudo-differential pair**

$$R_{TL} = 0$$

$$CMRR = 1$$

$$CMRR = 0 \text{ , dB.}$$



(a) R_{TL}=0, R_{e1}=0, R_{e2}=0
R_{TL}=0, R_{s1}=0, R_{s2}=0

(b) R_{TL} =0, $R_{e1}\neq 0$, $R_{e2}\neq 0$
R_{TL} =0, $R_{s1}\neq 0$, $R_{s2}\neq 0$

Figure 6.25 Pseudo-differential pair.

o Improvement of CMRR

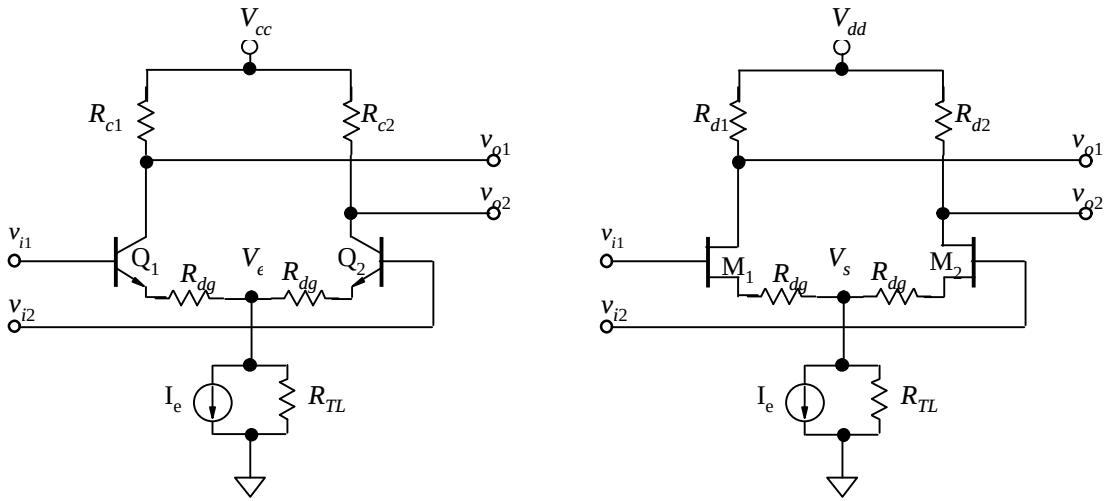


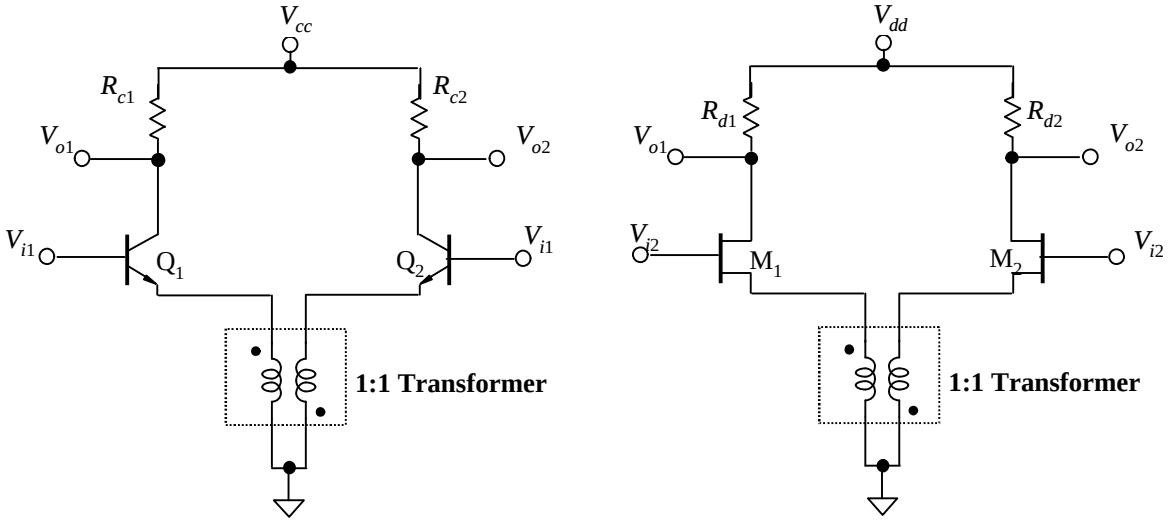
Figure 6.26 Emitteror sourcecoupled pair with degeneration resistors

$$A_{dm} = \frac{-g_m R}{1 + g_m R_{dg}\left(1 + \dfrac{1}{g_m R_{pgs}}\right)}$$

$$A_{cm} \approx \frac{-g_m R}{1 + 2g_m R_{TL}\left(1 + \dfrac{1}{g_m R_{pgs}}\right)\left(1 + \dfrac{R_{dg}}{2R_{TL}}\right)}$$

$$CMRR \approx \frac{A_{dm}}{A_{cm}} = \frac{1 + 2g_m R_{TL}\left(1 + \dfrac{1}{g_m R_{pgs}}\right)\left(1 + \dfrac{R_{dg}}{2R_{TL}}\right)}{1 + g_m R_{dg}\left(1 + \dfrac{1}{g_m R_{pgs}}\right)}$$

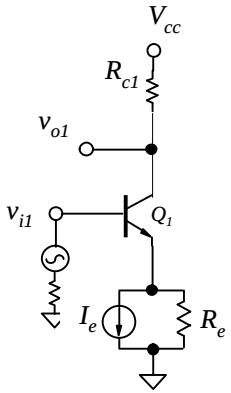
o Improvement of CMRR (Continued)



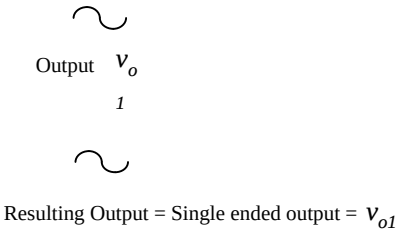
(a) Bipolar device (b) MOSFET

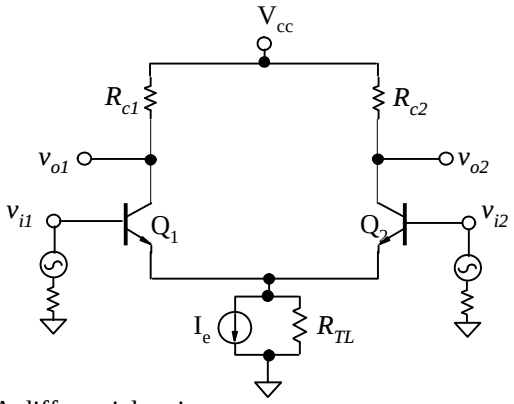
Figure 6.27 Improvement of CMRR by a 1:1 transformer

o Increase of voltage swing



(a) A single-ended amplifier.





(b) A differential pair.

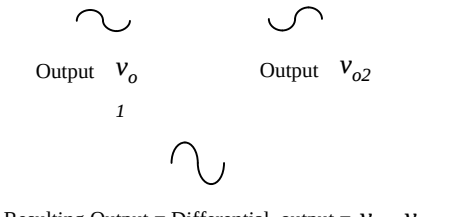
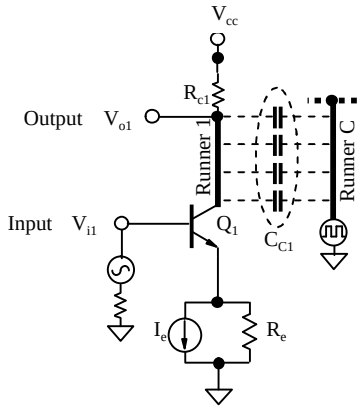
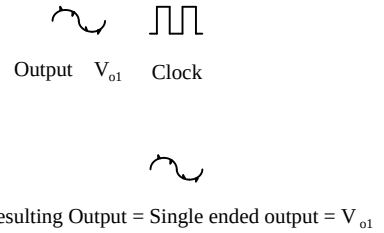


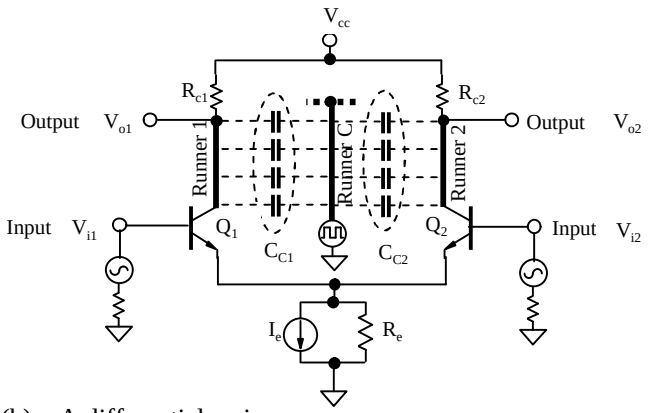
Figure 6.28 Increase of voltage swingin a differential pair

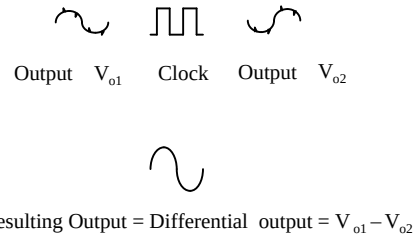
o Interference cancellation





(a) A single-ended amplifier.





(b) A differential pair.

Figure 6.29 Interference cancellation in a differential pair

o Interference cancellation (Continued)

- **Figure 4.27 shows that a differential pair can reject the interference but no "common mode noise" .**

- **Noise is a random stochastic process.**
  It is nonsense to talk about "common mode noise" or "differential mode noise"

- **A differential pair rejects interference partially**

  if the differential pair is in an imperfect symmetrical condition.

  A differential pair rejects interference from outside totally

  if the differential pair is in a perfect symmetrical condition.

oIncrease of noise

* **Noise can never be cancelled due to its differential function ina differential pair.**
* **Noise figure of a differential pair is about 3 dB more than that of a single-ended branch.**

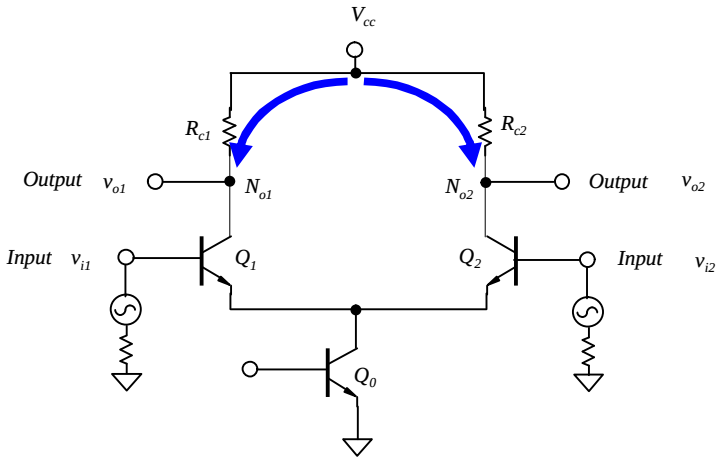


Figure 6.30 At differential outputs, noise from DC power supply cannot be“differentiated away”!

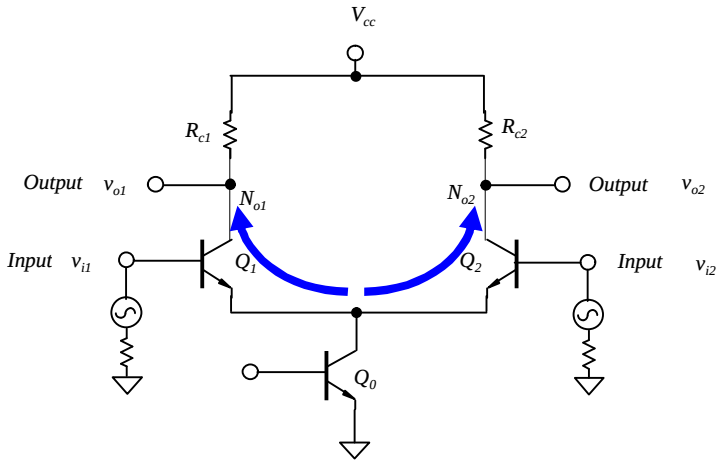
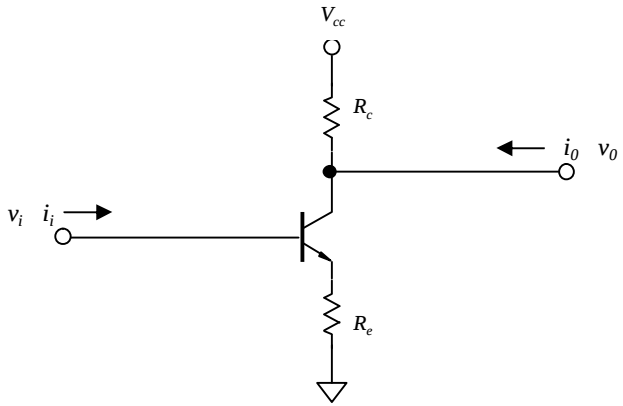


Figure 6.31 At differential outputs, noise from Q_0 cannot be “differentiated away”!

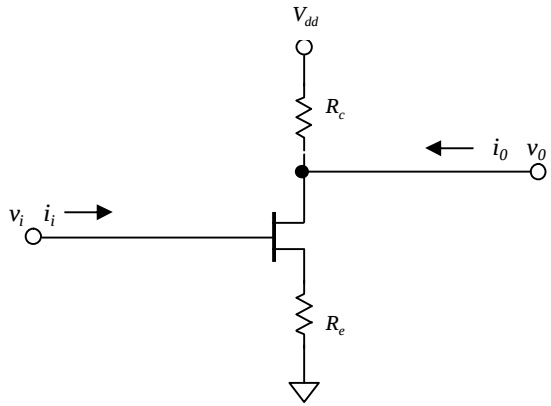
Reasons:

- **Two devices, Q1 and Q2, can be equivalent to two resisters, R_{c1} and R_{c2}.**
- **Then, by the same reasons as described in the previous problem, the process that these two devices attenuate or magnify the noise from Q_0 is a random stochastic process also.**
- **It is therefore concluded that it is impossible to keep attenuated or magnified noise exactly the same at two differential output terminals, V_{01} and V_{02}.**

3. Apparent difference between single ended and differential stage

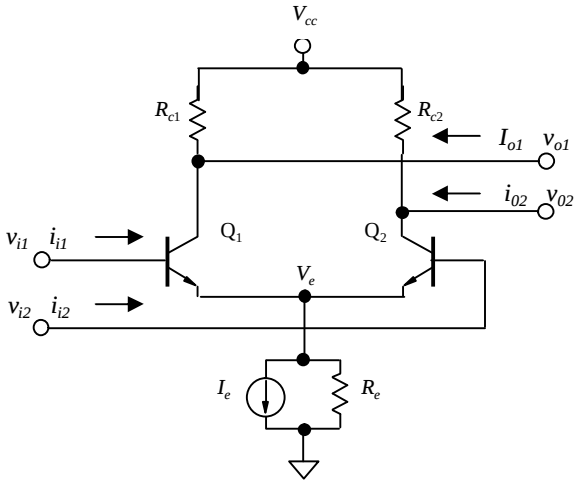


(a) A bipolar single-ended block

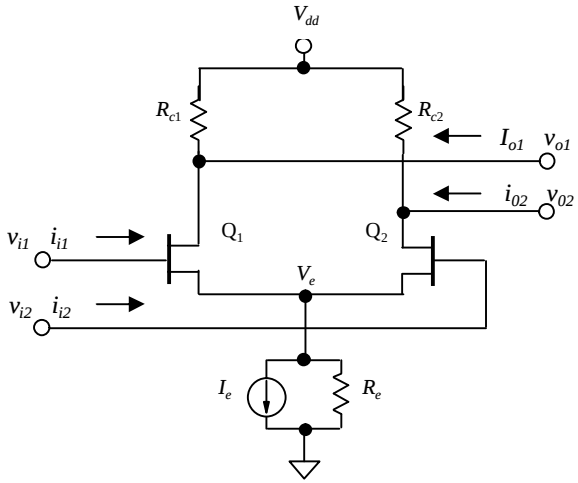


(b) A CMOS single-ended block

Figure 6. 32 Single-ended block



(a) A bipolar differential pair



(b) A CMOS differential pair

Figure 6. 33 Differential pair .

o Definition of a differential pair:

$v_{i1} = -v_{i2}$ or $|v_{i1}| = |v_{i2}|$, $\angle v_{i1} - \angle v_{i1} = 180^o$

$i_{i1} = -i_{i2}$ or $|i_{i1}| = |i_{i2}|$, $\angle i_{i1} - \angle i_{i2} = 180^o$

$v_{o1} = -v_{o2}$ or $|v_{o1}| = |v_{o2}|$, $\angle v_{o1} - \angle v_{o1} = 180^o$

$i_{o1} = -i_{o2}$ or $|i_{o1}| = |i_{o2}|$, $\angle i_{o1} - \angle i_{o2} = 180^o$

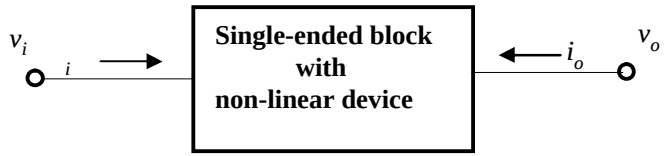
o Apparent difference between single ended block and differential pair

Table 5.4 Apparent difference between single ended block and differential pair

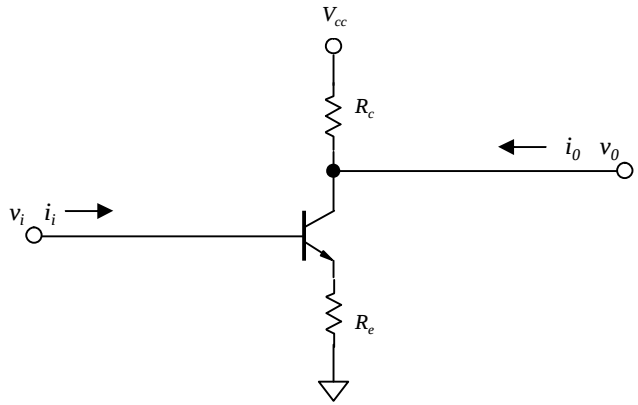
	Single-ended	Differential
Current drain	**1x**	**2x**
Layout area	**1x**	**2x**
Symmetry	**No**	**Yes**
DC offset (In deal case)	**Yes**	**No (Ideal)**
CMRR (In deal case)	**1**	**Infinitive (Ideal)**

4. DC offset

o DC offset (In deal case) is formed by a single-ended device



(a) Block diagram



(b) Schematic

Figure 6.34 A single-ended block with non-linear device

$V_{in} = V_i \sin \omega t$

$I_{out} = a_1 V_{in} + a_2 V_{in}^2 + a_3 V_{in}^3 + a_4 V_{in}^4 + \ldots\ldots$

$= a_1 V_i \sin \omega t + a_2 V_i^2 \sin^2 \omega t + a_3 V_i^3 \sin^3 \omega t + a_4 V_i^4 \sin^4 \omega t + \ldots\ldots$

$= a_1 V_i \sin \omega t + a_2 V_i [1-\cos 2\omega t]/2 + a_3 V_i^3 [3\sin \omega t - \sin 3\omega t]/4 + a_4 V_i^4 [3-4\cos 2\omega t + \cos 4\omega t]/8 +$

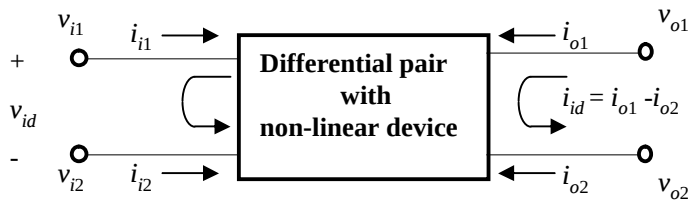
$\ldots\ldots$

$= a_1 V_i \sin \omega t - a_2 V_i^2 [\cos 2\omega t]/2 + a_3 V_i^3 [3\sin \omega t - \sin 3\omega t]/4 + a_4 V_i^4 [-4\cos 2\omega t + \cos 4\omega t]/8 + a_2 V_i^2 /2 + 3a_4 V_i^4 /8 + \ldots\ldots$

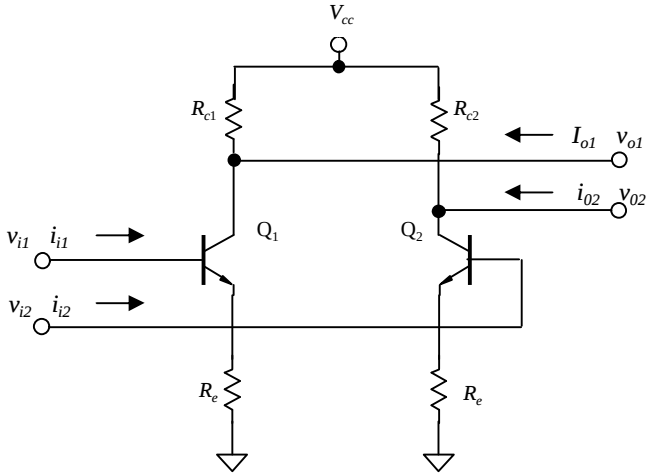
$I_{out,\ DC\text{-}offset} = a_2 V_i^2 /2 + 3a_4 V_i^4 /8 + \ldots\ldots$

DC offset is contributed by the even order non-linearity of the device.

o DC offset (In deal case) caused by a pair of devices



(a) Block diagram



(b) schematic

Figure 6.35 A differential pair with non-linear devices without coupling

$$V_{id} = V_{i1}\sin\omega t - V_{i2}\sin(\omega t+180^o)$$

$$I_{od} = I_{o1} - I_{o2}$$

$$I_{o1} = a_1V_{i1}\sin\omega t + a_2V_{i1}^2\sin^2\omega t + a_3V_{i1}^3\sin^3\omega t + a_4V_{i1}^4\sin^4\omega t + \ldots\ldots$$
$$= a_1V_{i1}\sin\omega t - a_2V_{i1}^2[\cos2\omega t]/2 + a_3V_{i1}^3[3\sin\omega t - \sin3\omega t]/4 + a_4V_{i1}^4[-4\cos2\omega t + \cos4\omega t]/8 +$$
$$a_2V_{i1}^2/2 + 3a_4V_{i1}^4/8 + \ldots\ldots$$

$$I_{o2} = -a_1V_{i2}\sin\omega t + a_2V_{i2}^2\sin^2\omega t - a_3V_{i2}^3\sin^3\omega t + a_4V_{i2}^4\sin^4\omega t + \ldots\ldots$$
$$= -a_1V_{i2}\sin\omega t + a_2V_{i2}^2[\cos2\omega t]/2 - a_3V_{i2}^3[3\sin\omega t - \sin3\omega t]/4 + a_4V_{i2}^4[-4\cos2\omega t + \cos4\omega t]/8 +$$
$$a_2V_{i2}^2/2 + 3a_4V_{i2}^4/8 + \ldots\ldots$$

If $V_{i1} = V_{i2} = V_{in,}$ then,

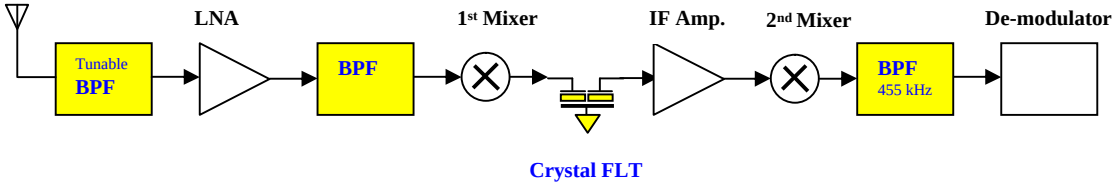
$$I_{od} = I_{o1} - I_{o2}$$
$$= 2a_1V_{in}\sin\omega t + 2a_3V_{i2}^3[3\sin\omega t - \sin3\omega t]/4 + \ldots\ldots$$

$I_{out,\ DC\text{-}offset} = 0$

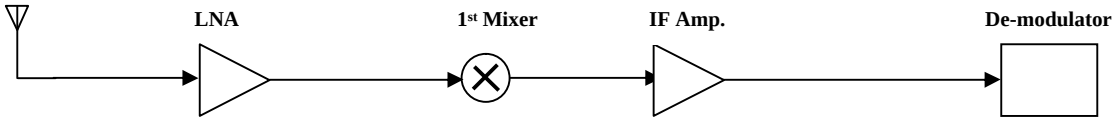
DC offset is zero due to the differential configuration.

o Why "zero" IF or direct conversion ?

* **In order to reduce the cost down, Zero-IF system replaces dual conversion system.**



(a) Dual conversion receiver



(b) Direct conversion receiver

Figure 6.36 Block diagram of dual conversion and direct conversion receiver

* **Zero-IF system hurt by DC-offset**
* **DC-offset = 0 in a differential pair.**

o DC offset cancellation

*** "Chopping" mixer**

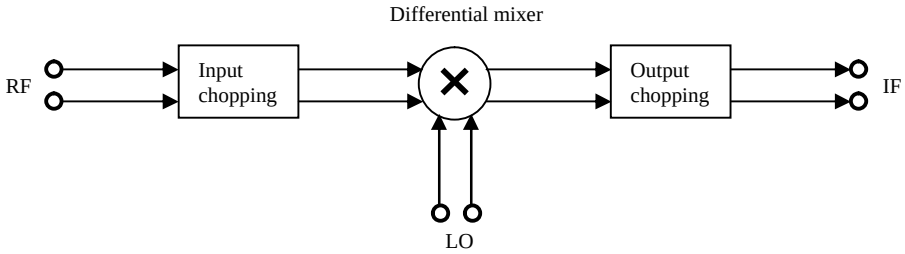
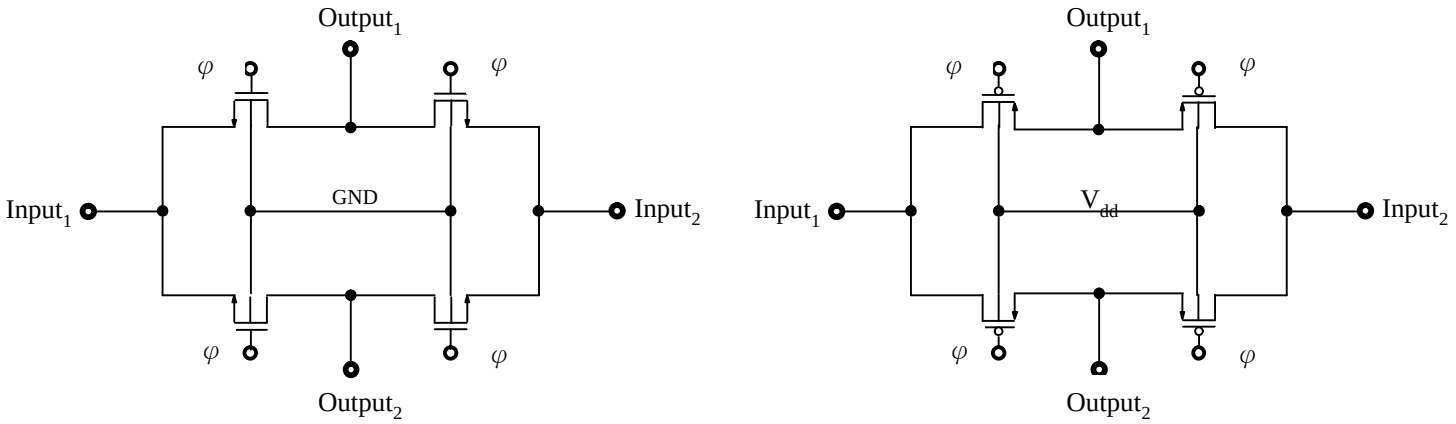


Figure 6.37 Block diagram of a "chopping" mixer



(a) Input chopping block (b) Output chopping block

Figure 6.38 Input and output chopping block of a "chopping" mixer

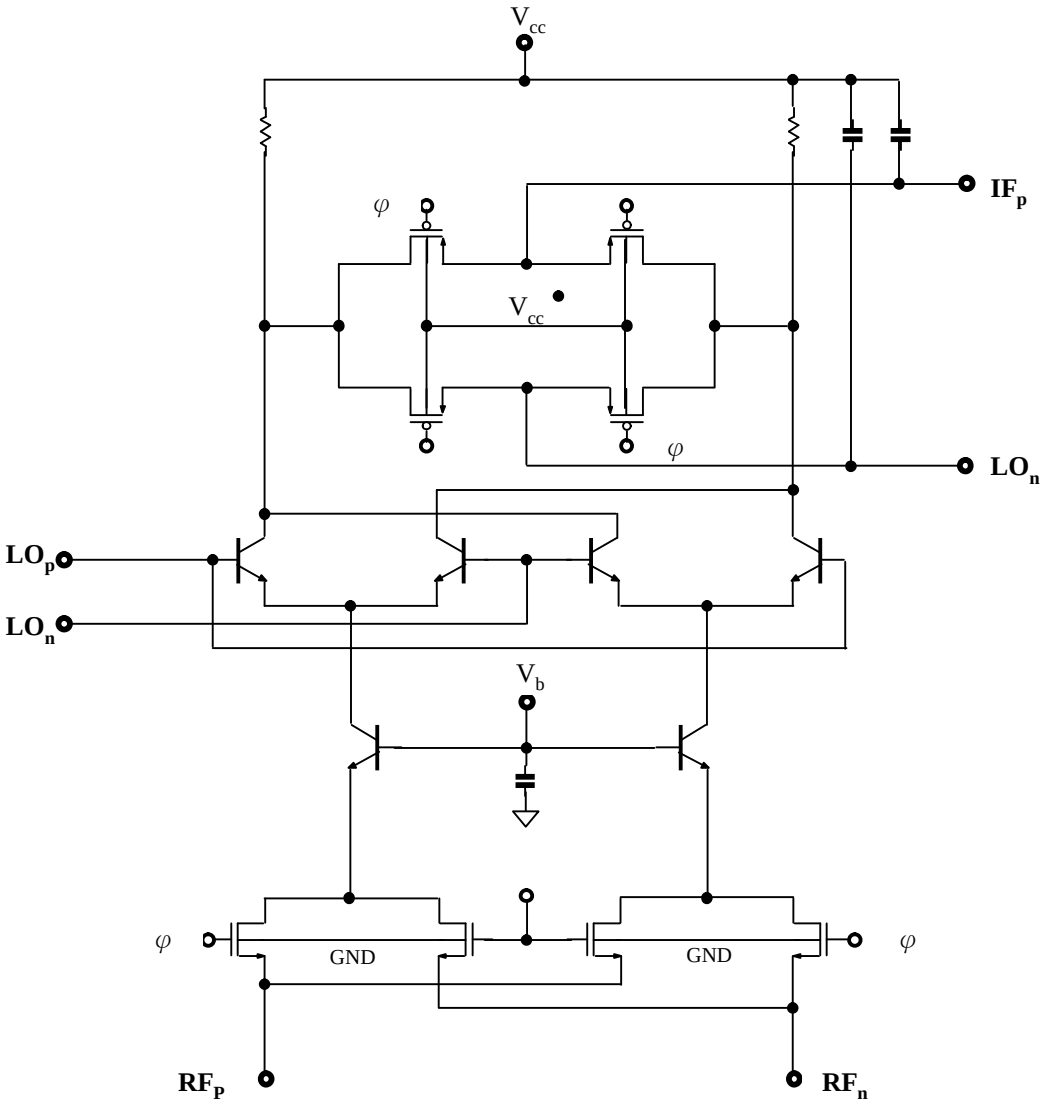


Figure 6.39 Topology of a "chopping" mixer

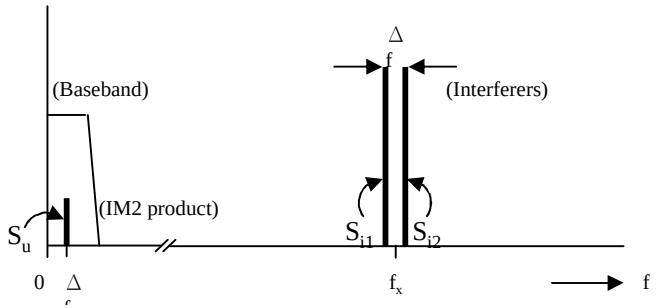


Figure 6.40 Two interferers result an un-desired IP2 product in a mixer.

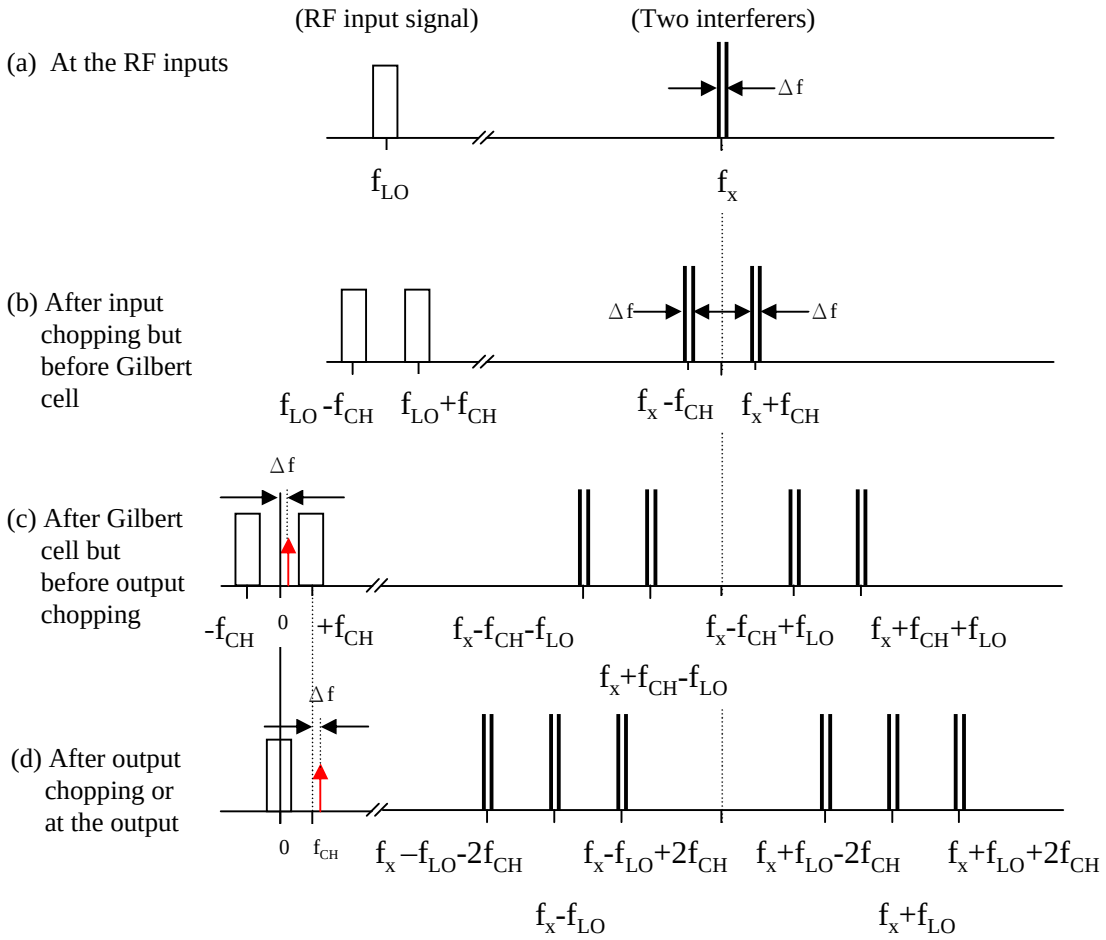


Figure 6.41 Principle of DC offset reduction in the "Chopping" mixer

* **DC offset calibration**

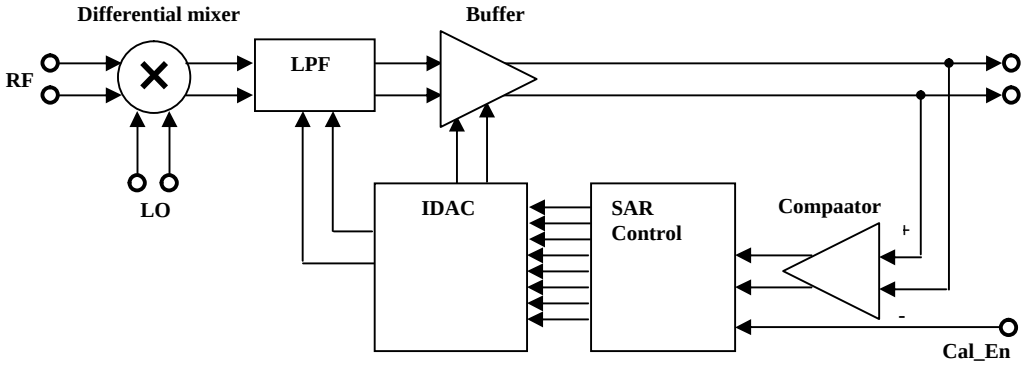


Figure 6.42 Block diagram of DC offset calibration

(SAR: Successive Approximation Register)

* **Hardware scheme**

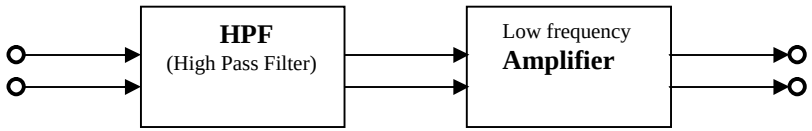


Figure 6.43 DC offset cancelled by the combination of a low frequency amplifier and a LPF.

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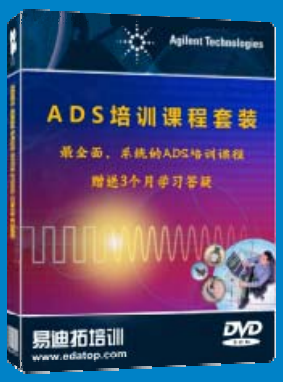

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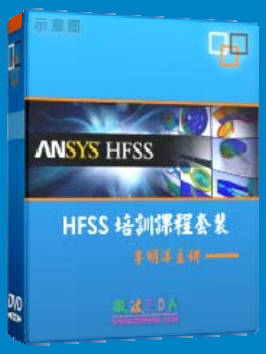

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