



## DESCRIPTION

The PT4303 is a low power super-heterodyne OOK/ASK receiver for the 315/434 MHz frequency bands. It offers a high level of integration and requires only few external components. The PT4303 consists of a low-noise amplifier (LNA), a down-conversion mixer, an on-chip phase-locked loop (PLL) with integrated voltage-controlled oscillator (VCO) and loop filter, an OOK/ASK demodulator, a data filter, a data slicing comparator and an on-chip regulator.

The PT4303 is available in 14-pin SOP package and is specified over the extended temperature range (-40 to +85°C).

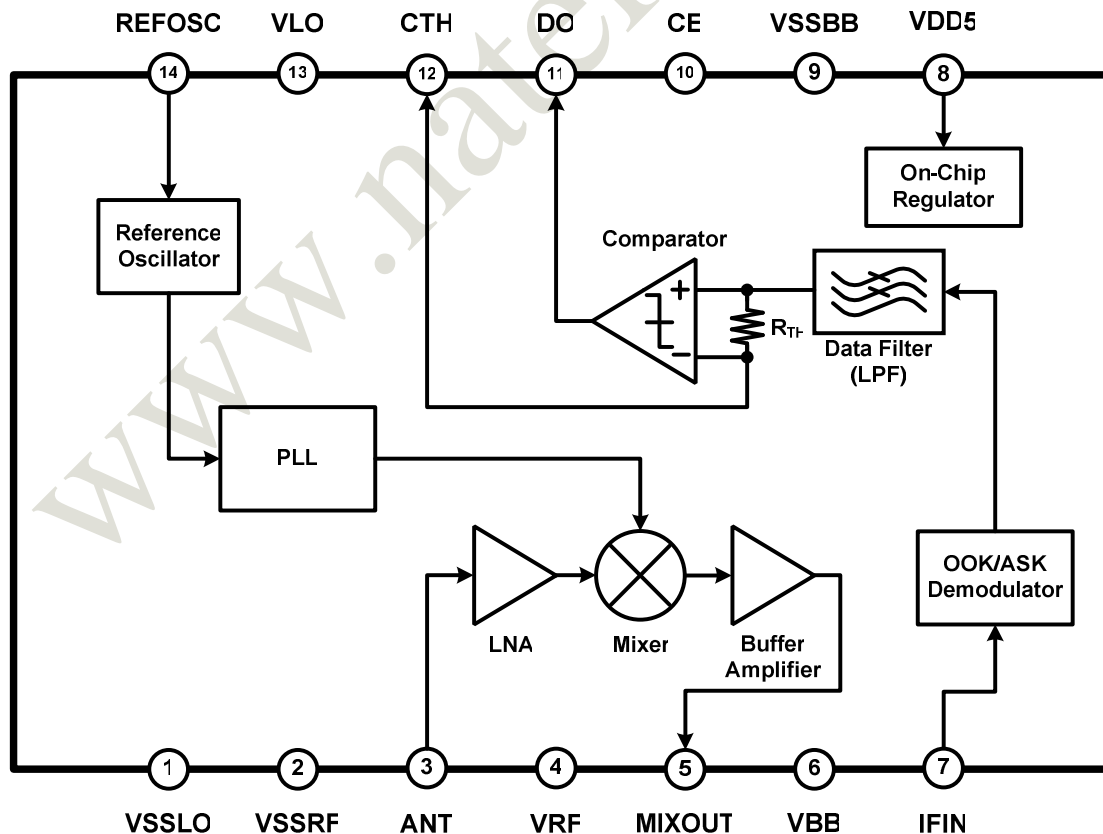
## FEATURES

- Ultra-low power consumption: 2.7 mA for fully operation (315 MHz)
- Few external components
- Excellent Sensitivity of the order of -110 dBm (peak ASK signal level at 315 MHz)
- Supply voltage range from 2.4 V to 5.5 V
- 250 MHz to 500 MHz frequency range
- Data rate up to 10 Kb/s

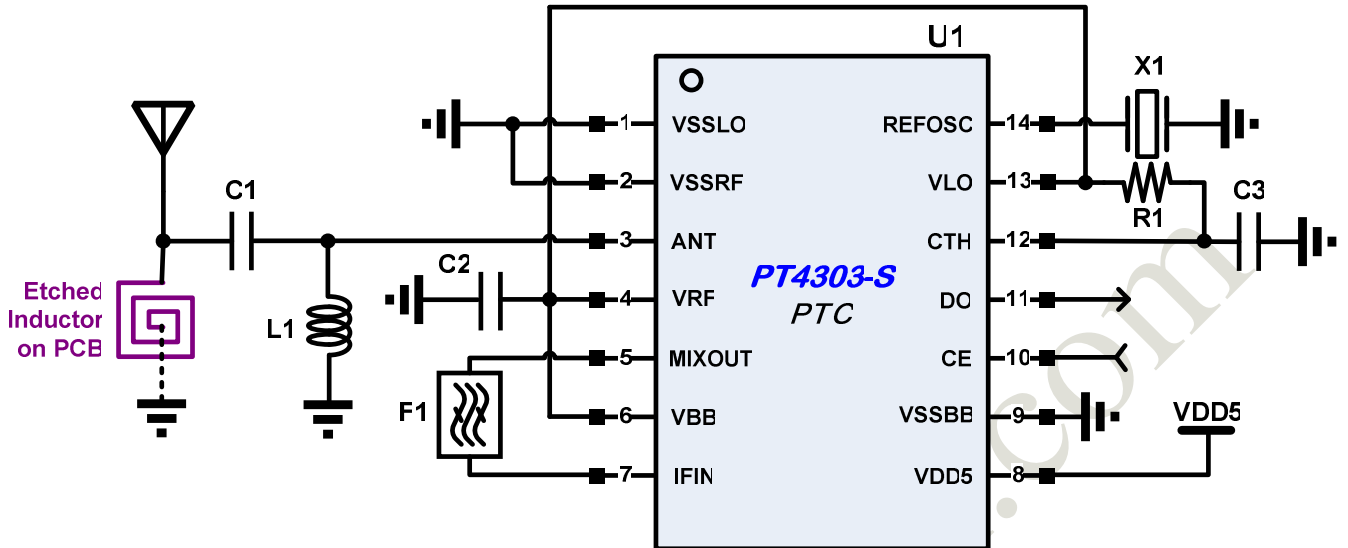
## APPLICATIONS

- Automotive Remote Keyless Entry (RKE)
- Remote Control
- Garage door and gate openers
- Suitable for circuit applications that meet either the European ETSI-300-220 or the North American FCC (Part 15) regulatory standards

## BLOCK DIAGRAM



## APPLICATION CIRCUIT



## BILL OF MATERIALS

Part	Value		Unit	Description
	315 MHz	433.92 MHz		
L1	82 n	47 n	H	Antenna input matching, coil inductor.
C1	1.8 p	1.0 p	F	Antenna input matching.
C2	100 n	100 n	F	Power supply de-coupling capacitor.
C3	470 n	470 n	F	$C_{TH}$ , affect coding type and start-up time.
R1	8.2 M	8.2 M	$\Omega$	For reducing data output noise (option).
F1	10.7	10.7	MHz	Band-pass filter.
X1	9.509	13.226	MHz	Reference crystal oscillator.
U1	PT4303 IC	PT4303 IC	U1	Receiver chip.

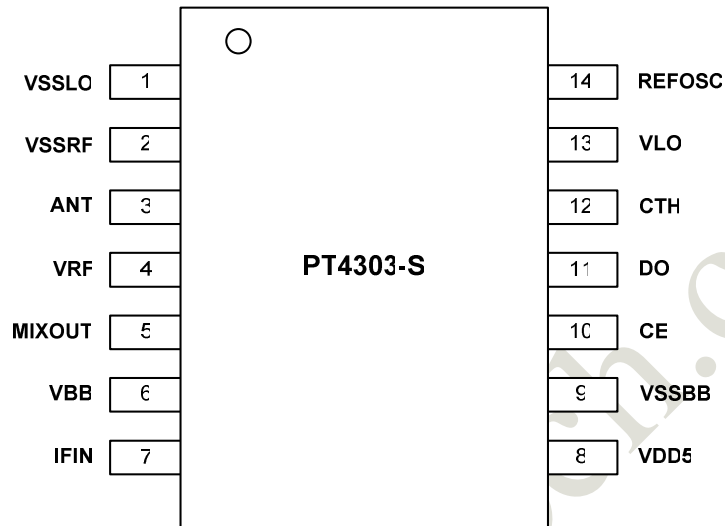
Notes:

1. L1 and C1 are the components for input matching network. They may have to be adjusted with different PCB layout and antenna requirement.
2. The value of C3 depends upon the data rate and coding pattern.
3. F1 is the 10.7 MHz ceramic filter. The recommended part number is Murata SFELA10M7HA00-B0.
4. The "option" components are based on application requirements.

## ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT4303-S	14 Pins, SOP, 150 mil	PT4303-S

## PIN CONFIGURATION



## PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
VSSLO	G	Ground for LO portion	1
VSSRF	G	Ground for RF portion	2
ANT	I	RF input connected to antenna by a matching network	3
VRF	P	Supply voltage for RF portion	4
MIXOUT	O	Mixer IF output	5
VBB	P	Supply voltage for baseband chain	6
IFIN	I	IF stage input	7
VDD5	P	5 V voltage regulator input	8
VSSBB	G	Ground for baseband chain	9
CE	I	Chip enable pin. Pull high to enable the chip	10
DO	O	Data output	11
CTH	I/O	Connect to data slicing threshold capacitor	12
VLO	P	Supply voltage for LO portion	13
REFOSC	I	Reference oscillator input pin	14



## ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage Range	$V_{DD5}$	-0.3	6	V
Analog I/O Voltage	–	-0.3	3	V
Digital I/O Voltage	–	-0.3	6	V
Operating Temperature Range	$T_A$	-40	+85	°C
Storage Temperature Range	$T_{STG}$	-55	+125	°C

## PACKAGE THERMAL CHARACTERISTIC

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
From Chip Junction Dissipation to External Environment	Rja	$T_A=27^\circ\text{C}$	–	37.15	–	°C/W
From Chip Junction Dissipation to Package Surface	Rjc		–	1	1.8	

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## ELECTRICAL CHARACTERISTICS

Nominal conditions:  $V_{DD5} = 5.0\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , CE = "High",  $T_A = +27^\circ\text{C}$ ,  $f_{RF} = 315\text{ MHz}$ ,  $f_{REFOSC} = 9.509\text{ MHz}$ .

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
<b>General Characteristics</b>						
Supply Voltage	$V_{DD5}$	Connect the supply voltage to VDD5 pin only	2.4	5.0	5.5	V
Current Consumption	$I_{DD5}$	$f_{RF}=315\text{ MHz}$	–	2.7	3.0	mA
		$f_{RF}=434\text{ MHz}$	–	2.9	3.2	
Standby Current	$I_{STBY}$	CE="Low"	–	–	1	$\mu\text{A}$
Operating Frequency Range	$f_{RF}$		250	–	500	MHz
Maximum Receiver Input Level	$P_{RF,MAX}$		-20	-15	–	dBm
Sensitivity <sup>1</sup>	$S_{IN}$	ASK <sup>2</sup> , $D_{Rate} = 2\text{ Kb/s}$ , Peak power level @ 315 MHz	–	-110	-107	dBm
		OOK, $D_{Rate} = 2\text{ Kb/s}$ , Peak power level @ 315 MHz	–	-104	-101	
		ASK <sup>2</sup> , $D_{Rate} = 2\text{ Kb/s}$ , Peak power level @ 434 MHz	–	-109	-106	dBm
		OOK, $D_{Rate} = 2\text{ Kb/s}$ , Peak power level @ 434 MHz	–	-103	-100	
Data Rate	$D_{RATE}$		–	2	10	Kb/s
LO Leakage	$L_{LO}$	Measured at antenna input	–	–	-80	dBm
System Start-Up Time	$T_{STUP}$	RF input power = -60 dBm	–	5	8	ms
<b>RF Front-End</b>						
Voltage Conversion Gain	$GV_{RF}$	Matched to $50\ \Omega$ @ 315 MHz	40	43	46	dB
		Matched to $50\ \Omega$ @ 434 MHz	39	42	45	
Noise Figure	$NF_{RF}$	Matched to $50\ \Omega$ @ 315 MHz	–	5.7	6.3	dB
		Matched to $50\ \Omega$ @ 434 MHz	–	6.1	6.7	
Mixer Output Impedance	$Z_{OUT,MIXER}$	Measured at MIXOUT pin	300	330	360	$\Omega$
<b>IF Section</b>						
IF Frequency	$f_{IF}$		–	10.7	–	MHz
IF Bandwidth	$BW_{IF}$	Depends on the external ceramic filter	–	180	–	KHz
IF Input Impedance	$Z_{IN,IF}$		300	330	360	$\Omega$
<b>Demodulator</b>						
CTH Leakage Current	$I_{ZCTH}$	$T_A = +85^\circ\text{C}$	–	$\pm 100$	–	nA
<b>Phase-Locked Loop</b>						
Reference Frequency	$f_{REFOSC}$		7	–	16	MHz
Reference Signal Voltage Swing	$V_{REF}$	Peak-to-peak voltage ( $V_{PP}$ )	0.3	–	1.5	V
VCO Frequency Range	$f_{VCO}$		220	–	550	MHz
Divider Ratio	DIV		–	32	–	–
<b>Digital/Control Interface</b>						
Input-High Voltage	$V_{IN,High}$	CE, SELA, SELB pins	0.8	–	–	$V_{DD5}$
Input-Low Voltage	$V_{IN,Low}$	CE, SELA, SELB pins	–	–	0.2	$V_{DD5}$
Output Current	$I_{OUT}$	DO pin, push-pull	–	20	–	$\mu\text{A}$
Output-High Voltage	$V_{OUT,High}$	DO pin, $I_{OUT} = -1\ \mu\text{A}$	0.9	–	–	$V_{DD5}$
Output-Low Voltage	$V_{OUT,Low}$	DO pin, $I_{OUT} = +1\ \mu\text{A}$	–	–	0.1	$V_{DD5}$
Output Rise/Fall Times	$t_R / t_F$	DO pin, $C_{LOAD} = 15\text{ pF}$	–	10	–	$\mu\text{s}$

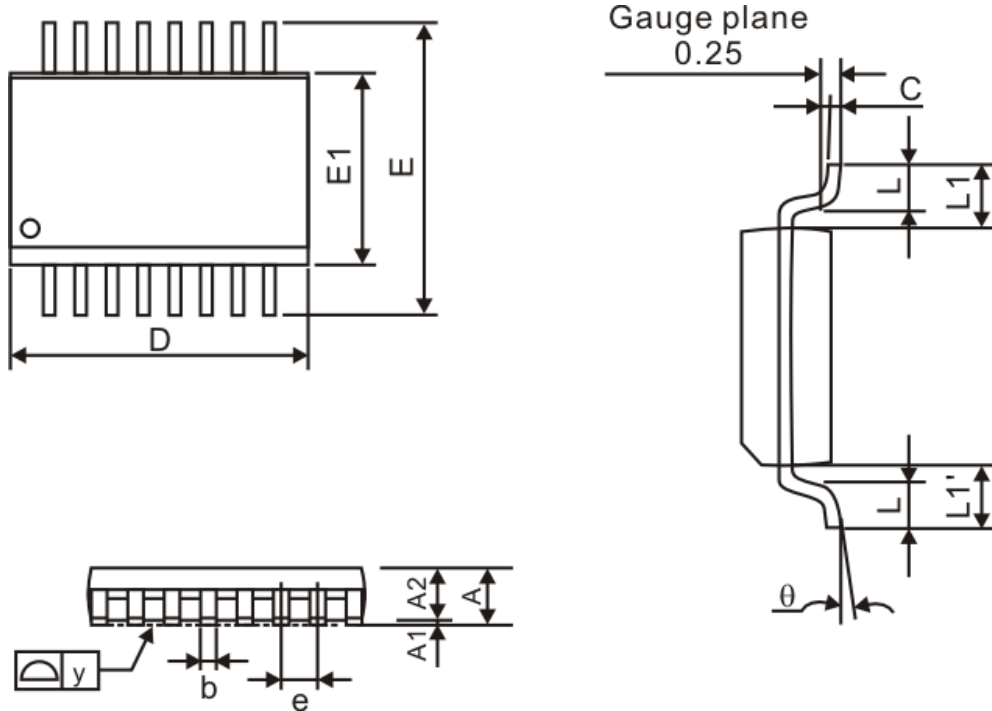
Notes:

1. BER =  $1e-3$
2. AM 99% with square-wave modulation



## PACKAGE INFORMATION

14 PINS, SOP, 150 MIL



Symbol	Min.	Nom.	Max.
A	1.35	1.60	1.75
A1	0.10	-	0.25
A2	-	1.45	-
b	0.33	-	0.51
C	0.19	-	0.25
D	8.55	-	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	-	1.27	-
L	0.40	-	1.27
L1	1.04REF		
y	-	-	0.10
θ	0°	-	8°

Notes:

1. Refer to JEDEC MS-012.
2. Unit: mm



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