Revision March 2004

AR2112 Multi-Mode, Radio-on-a-Chip for IEEE 802.11b/g Wireless LANs

General Description

The Atheros AR2112 iMs part of the two-chip AR5002G and AR5002AP-G solutions for IEEE 802.11b/g (2.4 GHz) wireless local area networks (WLANs). When combined with the AR5212 or AR2312, these chip sets enable a high performance, low cost, compact solution that easily fits onto one side of a PC Card, Mini PCI Card, or access point applications.

The AR2112 operates in the 2.4 GHz frequency bands:

Freq	Bands	Frequency
2.4 GHz		2.312 – 2.472 GHz 2.484 GHz

The transmitter combines baseband in-phase (I) and quadrature (Q) signals, up-converts them to the desired frequency channel, and drives the RF signal off-chip through the integrated power amplifier.

The receiver uses an integrated dual conversion architecture and requires no off-chip intermediate frequency (IF) filters.

The frequency synthesizer operates with 5 MHz steps to match the frequency channels defined by IEEE 802.11b/g as well as supporting the Atheros Super G™ mode. An on-chip crystal oscillator allows clock generation with a single external crystal configuration.

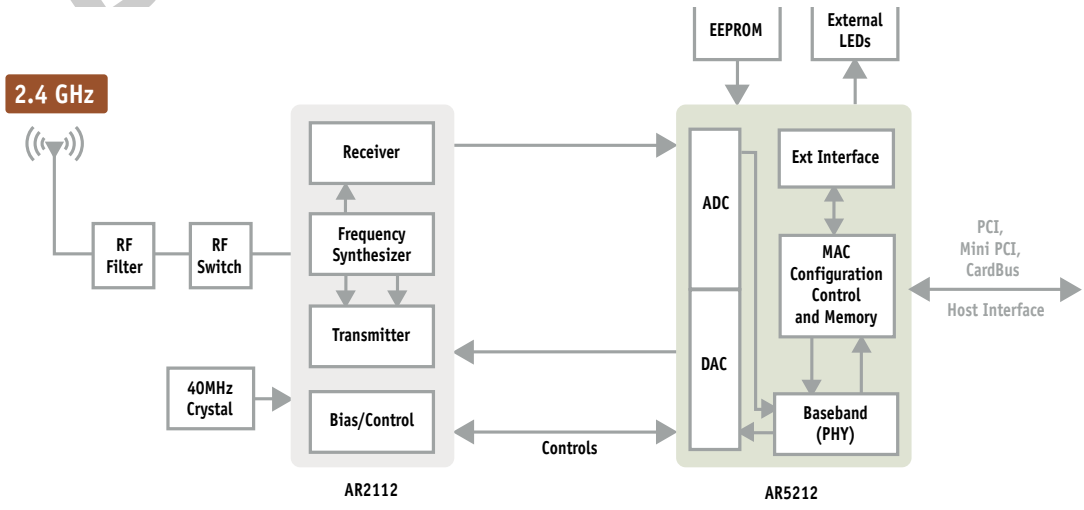
The transmitter, receiver, and frequency synthesizer functions are controlled using the AR5212 or AR2312 through a serial programming bus and on-chip control registers.

All internal bias currents are generated on-chip with a single external reference resistor.page

Features

- Radio chip for the Atheros IEEE 802.11b/g radio
- No external VCOs and SAW filters needed
- 64-pin leadless plastic chip carrier package
- Together with the AR5212 MAC/Baseband processor, or the AR2312 Wireless System-on-a-Chip (WiSoC):
  - IEEE 802.11b/g compatible
  - Low power operating and sleep mode

AR5002G System Block Diagram



1. Pin Descriptions

This section contains a package pinout and a tabular listing of the signal descriptions.

The following nomenclature is used for signal names:

- NC indicates no connection should be made to this pin. See Table 1-1 for details.
- _L at the end of the signal name indicates active low signals.
- p at the end of the signal indicates the positive side of a differential signal.
- n at the end of the signal indicates the negative side of a differential signal.

The following nomenclature is used for signal types described in Table 1-1:

- IA indicates an analog input.
- I indicates a digital input.
- OA indicates an analog output.
- O indicates a digital output.
- P indicates a power/ground.

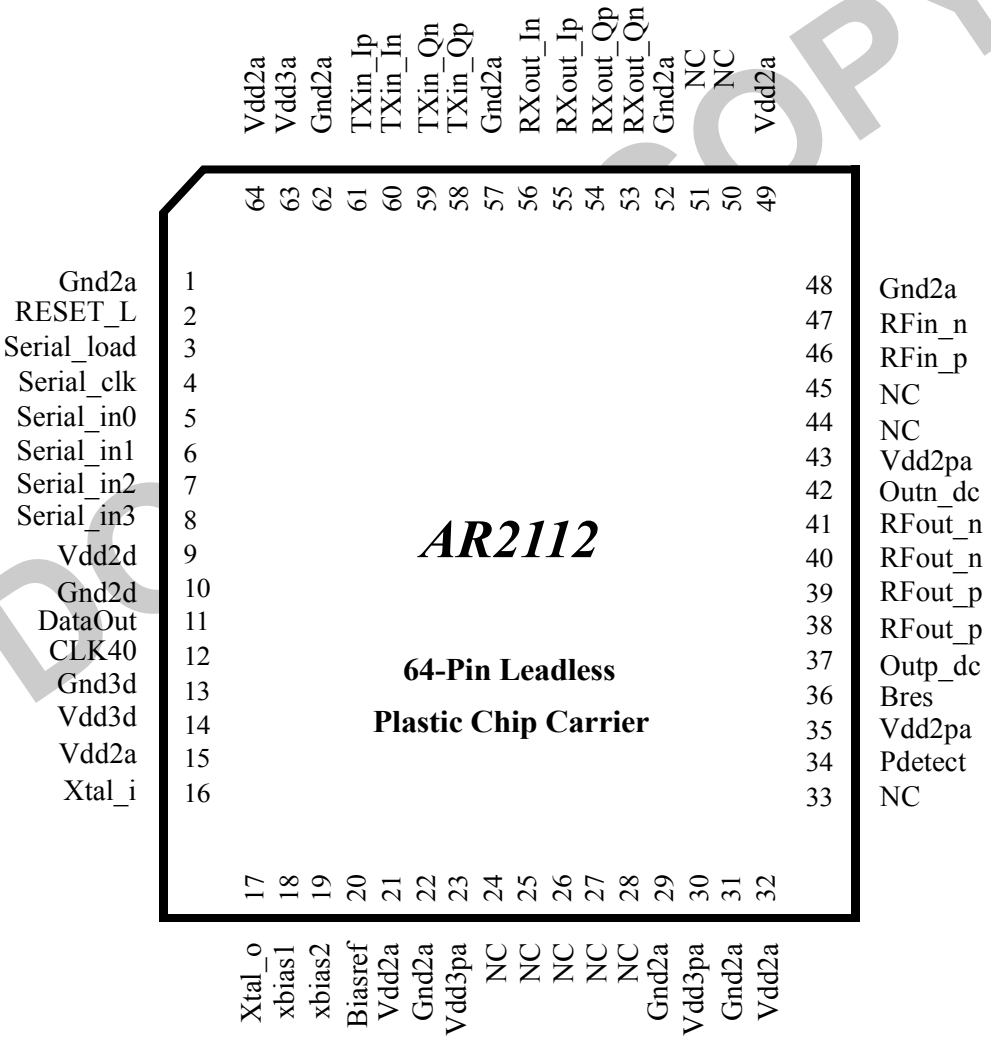


Figure 1-1. **Package Pinout (Top View)**

Table 1-1. **Signal to Pin Relationships and Descriptions**

Symbol	Pin	Type	Source or Destination	Description
Receiver				
RFin_n	47	IA	RF input	Differential RF inputs at 2.4 GHz. Use one side for single-ended input.
RFin_p	46	IA	RF input	
RXout_Qn	53	OA	BB/WiSoC	Differential baseband I and Q outputs from the receiver to the MAC/Baseband processor or the WiSoC. Anti-aliasing filter is on-chip.
RXout_Qp	54	OA	BB/WiSoC	
RXout_In	56	OA	BB/WiSoC	
RXout_Ip	55	OA	BB/WiSoC	
Transmitter				
TXin_Qn	59	IA	BB/WiSoC	Differential baseband I and Q inputs from DAC on the MAC/Baseband processor or the WiSoC. Reconstruction filter is on-chip.
TXin_Qp	58	IA	BB/WiSoC	
TXin_In	60	IA	BB/WiSoC	
TXin_Ip	61	IA	BB/WiSoC	
RFout_n	41, 40	OA	RF output	Differential 2.4 GHz RF power amplifier outputs.
RFout_p	39, 38	OA	RF output	
Pdetect	34	I	—	External Envelope Detector Input for 2.4 GHz RF signal.
Outp_dc	37	I	Analog	2.4 GHz PA drain bias. 3.3 V bias.
Outn_dc	42	I	Analog	
Vdd2pa	43, 35	I	Analog 2.5 V	PA Vdd for the 2.4 GHz PA.
Vdd3pa	23, 30	I	Analog 3.3 V	PA Vdd for the 2.4 GHz PA driver.
Bres	36	I	—	3 kΩ Bias resistor to Vdd2a for 2.4 GHz PA
Bias/Control				
Xtal_i	16	I	40 MHz crystal	Crystal input and output.
Xtal_o	17	O	40 MHz crystal	
CLK40	12	O	BB/WiSoC	40 MHz reference clock. 3.3 V.
RESET_L	2	I	BB/WiSoC	Active low reset. Must be active for at least 500 ns., 3.3 V.
Serial_load	3	I	BB/WiSoC	Load for control shift register. 3.3 V.
Serial_clk	4	I	BB/WiSoC	Shift clock for control shift register. 3.3 V.
Serial_in0	5	I	BB/WiSoC	Input data for control shift register. 3.3 V.
Serial_in1	6	I	BB/WiSoC	Input data for control shift register. 3.3 V.
Serial_in2	7	I	BB/WiSoC	Input data for control shift register. 3.3 V.
Serial_in3	8	I	BB/WiSoC	Input data for control shift register. 3.3 V.
DataOut	11	0	BB/WiSoC	Digital Data Output Pin.
Biasref	20	I	6.19 kΩ	Reference pin for external bias resistor. 6.19 kΩ ± 1% to ground.

Table 1-1. **Signal to Pin Relationships and Descriptions (continued)**

Symbol	Pin	Type	Source or Destination	Description
xbias1	18	OA	Bias Output	General purpose analog bias pins.
xbias2	19	OA	Bias Output	
Power				
Vdd3a	63	P	3.3 V	Analog 3.3 V power supply for Synthesizer VCO.
Vdd2a	15, 21, 32, 49, 64	P	2.5 V	Analog 2.5 V power supply.
Vdd3d	14	P	3.3 V	Digital Vdd for 3.3 V pads.
Vdd2d	9	P	2.5 V	Digital 2.5 V Vdd for logic.
Gnd2a	1, 22, 29, 31, 48, 52, 57, 62	P	0 V	Analog ground.
Gnd2d	10	P	0 V	Digital ground for logic.
Gnd3d	13	P	0 V	Digital I/O ground.
Reserved				
NC	24-28, 33, 44-45, 50-51	I/O	—	Do Not Connect

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1 summarizes the absolute maximum ratings and Table 2-2 lists the recommended operating conditions for the AR2112. Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

Table 2-1. **Absolute Maximum Ratings**

Symbol	Parameter	Max. Rating	Unit
V_{dd2}	Supply voltage	–0.3 to 3.0	V
V_{dd3}	Maximum I/O supply voltage	–0.3 to 4.0	V
RF_{in}	Maximum RF input (reference to 50 Ω)	+10	dBm
T_{store}	Storage temperature	–65 to 150	°C
ESD	Electrostatic discharge tolerance	1500	V

2.2 Recommended Operating Conditions

Table 2-2. **Recommended Operating Conditions**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{dd2}	Supply voltage	± 5%[1]	2.375	2.5	2.625	V
V_{dd3}	I/O voltage	± 10%[1]	3.0	3.3	3.6	V
T_{case}	Case temperature	—	0	25	95	°C
T_j	Junction temperature	—	0	50	110	°C

[1]The recommended power-on sequence is to have V_{dd3} lag V_{dd2}.

2.3 AC Electrical Characteristics

The following conditions apply to all characteristics unless otherwise specified: V_{dd2} = 2.5 V, V_{dd3} = 3.3 V, T_{case} = 25 °C.

Unless otherwise specified, all measurements are to be performed with test circuits based on the reference design.

2.3.1 Receiver Characteristics

Table 2-3 summarizes the receiver characteristics for the AR2112.

Table 2-3. **Receiver Characteristics for 2.4 GHz operation**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F_{rx}	Receive input frequency range	5 MHz center frequency	2.312	—	2.484	GHz
NF	Receive chain noise figure	See Note [1]	—	5.5	—	dB
S_{rf}	Sensitivity CCK, 1 Mbps CCK, 11 Mbps OFDM, 6 Mbps OFDM, 54 Mbps	See Note [2]	 — — — —	 -95 -90 -92 -73	 — — — —	dBm
IP1dB	Input 1 dB compression (min. gain)	—	-12	-10	—	dBm
IIP3	Input 3rd intercept point (min. gain)	—	-3	-1	—	dBm
Z_{RFin_input}	Recommended LNA differential drive impedance	See Note [3]	—	9+j40	—	—
ER_{phase}	I,Q phase error		—	1.5	2	degree
ERamp	I,Q amplitude error		—	0.5	1	dB
R_{adj}	Adjacent channel rejection CCK OFDM, 6 Mbps OFDM, 54 Mbps	10 to 20 MHz See Note [4]	 35 16 –1	 24 7	 — — —	dB
BB_{atten}	Baseband filter attenuation 20 MHz offset 40 MHz offset		 — —	 -21 -46	 -17 -40	dB
BB_{ripple}	Baseband filter passband ripple	—	—	0.4	1	dB
TRpowup	Time for power up (from synth on)	—	—	1	—	µs

[1]Measured using the balun recommended by Atheros. An increase of 2 dB in noise figure is expected at 85°C. The use of an external LNA is recommended.
[2]Sensitivity performance is based on the Atheros reference design which includes RF filter, TX/RX antenna switch and an external LNA.
[3]Refer to the hardware design guide for information.
[4]Measured with AR5212.

2.3.2 Transmitter Characteristics

Table 2-4 summarizes the transmitter characteristics for the AR2112.

Table 2-4. **Transmitter Characteristics for 2.4 GHz operation**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F_{tx}	Transmit output frequency range	5 MHz center frequency	2.312	—	2.484	GHz
P_{out}	Mask Compliant CCK output power	T_{amb} = 25 °C See Note [1]	—	10	—	dBm
	EVM Compliant OFDM output power for 64QAM			6		dBm
SP_{gain}	PA gain step	See Note [2]	—	0.5	—	dB
A_{pl}	Accuracy of power leveling loop	See Note [3]	—	± 0.5	± 1.5	dB
Z_{RFout_load}	Recommended PA differential load impedance	See Note [4]	—	20 - j10	—	—
OP1dB	Output P1dB (max. gain) See note 3	2.442 GHz, 25 °C	13	15	—	dBm
OIP3	Output 3rd order intercept point (max. gain)	2.442 GHz, 25 °C	24	26	—	dBm
SS	Sideband suppression		—	–50	–30	dBc
C_{leak}	Carrier leakage	—	—	-35	-23	dBc
LO_{Harm}	LO Harmonics Center frequencies: 2.412 - 2.472 GHz 2.016 GHz 2.688 GHz Center frequency: 2.484 GHz 2.112 GHz 2.816 GHz	—	 — — — —	 55 55 45 50		dBc
RS	Synthesizer reference spur:	—	—	-55		dBc
Tx_{mask}	Transmit spectral mask CCK OFDM	 At 11 MHz offset At 22 MHz offset At 11 MHz offset At 20 MHz offset At 30MHz offset	 –30 -50 -20 -28 -51	 -35 -53 -27 -38 -52	 — — — — —	dBr
TTpowup	Time for power up (from synth on)	—	—	1.5	—	µs

[1]Measured using the balun recommended by Atheros under closed-loop power control. The use of an external PA with external power detector is recommended. See application notes on *External Power Control for Design Using AR5002*.
[2]Guaranteed by design.
[3]Manufacturing calibration required.
[4]Refer to the design guide for information.

2.3.3 Synthesizer Characteristics

Table 2-5 summarizes the synthesizer characteristics for the AR2112.

Table 2-5. **Synthesizer Composite Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Pn	Phase noise (at Tx_Out)	30 kHz offset	—	–105	-100	dBc/Hz
		100 kHz offset	—	–105	-100	dBc/Hz
		500 kHz offset	—	–105	-100	dBc/Hz
		1 MHz offset	—	–108	-103	dBc/Hz
F_c	Center channel frequency	Center frequency at 5 MHz spacing (see Note [1])	2.312	—	2.484	GHz
F_{ref}	Reference oscillator frequency	± 25 ppm	—	40	—	MHz
F_{step}	Frequency step size (at RF)	See Note [2]	—	5	—	MHz
TS_{powup}	Time for power up (from sleep)	—	—	0.2	—	ms

[1]Frequency is measured at the TX output.
[2]5 MHz channel spacing is for the 2.312 to 2.472 GHz band. 2.484 GHz is for use in Japan.

2.3.4 Power Consumption Parameters

The following conditions apply to the typical characteristics unless otherwise specified:

V_{dd2} = 2.5 V, V_{dd3} = 3.3 V, T_{amb} = 25 °C

Table 2-6 shows the typical power drain on each of the four on-chip power supply domains as a function of the AR2112's operating mode.

Table 2-6. **Power Consumption for 2.4 GHz Operation (All in milliWatts)**

Operating Mode	3.3 V Digital Supply (Vdd3d)	3.3 V Analog Supply (Vdd3pa, Vdd3a)	2.5 V Digital Supply (Vdd2d)	2.5 V Analog Supply (Vdd2a, Vdd2pa)	Total	Unit
Sleep (see Note [1])	0	0	0	6.25	6.25	mW
Tx (see Note [2])	9	345	8.75	350	712	mW
Rx (max. gain) (see Note [3])	9	47	8.75	305	370	mW

[1]Powered-down state; only the CLK40 pads and crystal oscillator are on.
[2]Transmitter and synthesizer are on.
[3]Receiver and synthesizer are on with maximum receive gain.

3. Functional Description

The AR2112 transceiver consists of four major functional blocks:

- Receiver (RX)
- Transmitter (TX)
- Frequency synthesizer (SYNTH)
- Associated bias/control (BIAS)

See Figure 3-1.

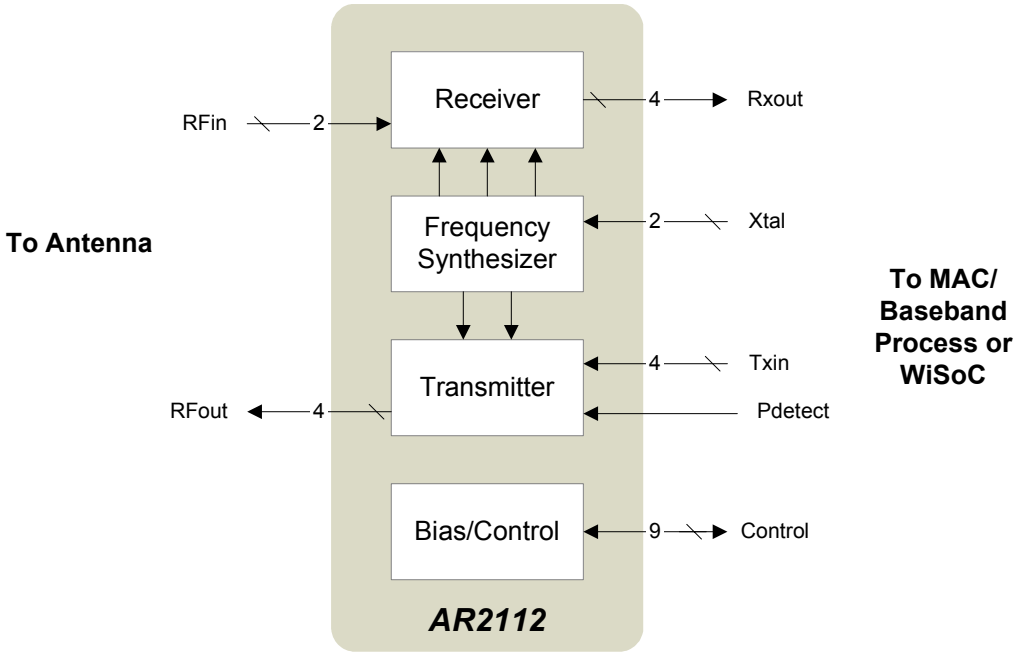


Figure 3-1. **AR2112 Functional Block Diagram**

3.1 Receiver (RX) Block

The receiver converts an RF signal (with 20 MHz or 40 MHz bandwidth) to baseband I and Q outputs. The input frequency range of the receiver is 2.4 GHz for IEEE 802.11b/g signals.

The receiver implements an integrated down-conversion architecture that eliminates the requirement for an external intermediate frequency filter, while providing the advantages of traditional heterodyne approaches. The receiver topology includes a low noise amplifier (LNA), a radio frequency (RF) mixer, an intermediate frequency (IF) mixer, and a baseband programmable gain amplifier (PGA) as shown in Figure 3-2. The RF mixer converts the output of the on-chip LNA to an intermediate frequency. The IF mixer converts this signal down to baseband I and Q signals. The I and Q signals are low-pass filtered and amplified by a baseband Programmable Gain Filtercontrolled by digital logic. The baseband signals are sent to the ADC of the MAC/Baseband processor or WiSoC.

The DC offset of the receive chain is reduced using multiple DACs controlled by the MAC/ Baseband processor or WiSoC. Additionally, the receive chain can be digitally powered down to conserve power.

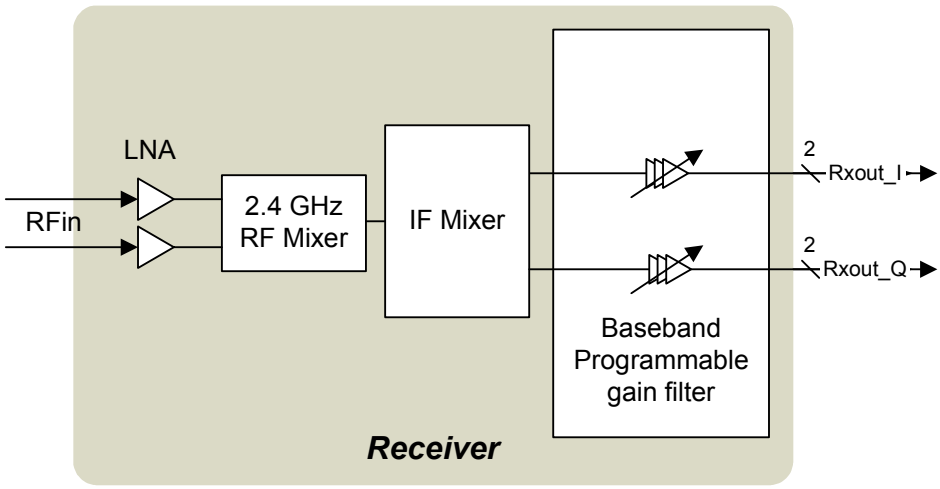


Figure 3-2. **RF Receiver Functional Block Diagram**

3.2 Transmitter (TX) Block

The transmitter converts baseband I and Q inputs to 2.4 GHz RF outputs as shown in Figure 3-3. The inputs of the transmitter are current outputs of the DAC in the AR5212. These currents are low-pass filtered through on-chip reconstruction filter to remove spectral images and out-of-band quantization noise. The I and Q signals are converted to RF signals using an integrated up-conversion architecture. The intermediate frequency (IF) mixer converts the baseband signals to an intermediate frequency. The radio frequency (RF) mixer converts the IF signals into radio frequency signals. These signals are driven off-chip through a power amplifier.

The transmit chain can be digitally powered down to conserve power. To ensure that the FCC limits are observed and output power stays close to the maximum allowed, the transmit output power is adjusted by a closed loop, digitally programmed, control loop at the start of each packet. The closed-loop power control can be based on either an on-chip or off-chip power detector. Refer to application notes *External power detection and predistortion* for more details.

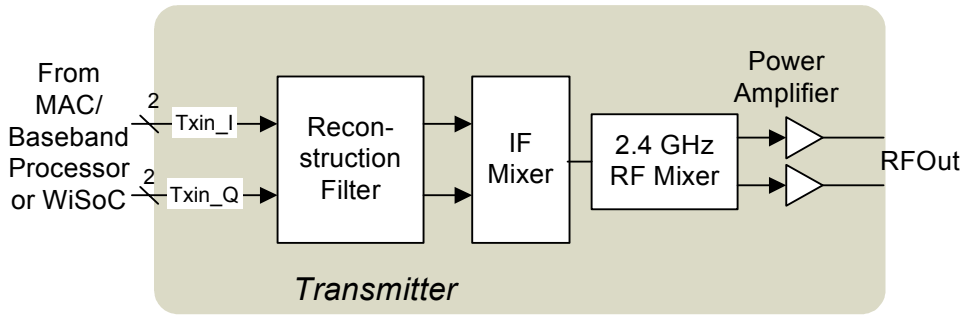


Figure 3-3. **RF Transmitter Functional Block Diagram**

3.3 Synthesizer (SYNTH) Block

The AR2112 supports two on-chip synthesizers to generate local oscillator (LO) frequencies for the receiver and transmitter mixers. Both synthesizers share the topology shown in Figure 3-4. A signal generated from a 40 MHz crystal is used as the reference input for the synthesizer. An on-chip voltage controlled oscillator (VCO) provides the desired LO signal based on a phase/frequency locked loop. The loop filter components are all integrated on chip and can be digitally optimized through the serial interface.

On power up or channel reselection, the synthesizer takes approximately 0.2 ms to settle.

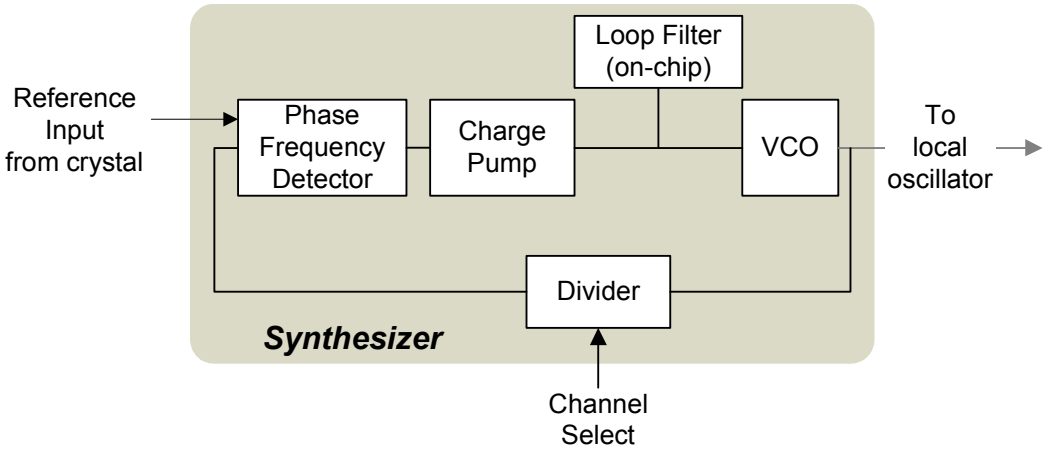


Figure 3-4. **RF Synthesizer Block Diagram**

3.4 Bias/Control (BIAS) Block

The bias/control block provides the reference voltages and currents for all other circuit blocks (see Figure 3-5). An on-chip bandgap reference circuit provides the needed voltage and current references based on an external 6.19 kΩ ± 1% resistor.

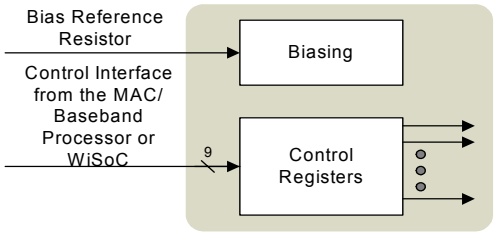


Figure 3-5. **Bias/Control Architecture**

The MAC/Baseband processor or WiSoC controls the state of the AR2112 through the control interface.

4. Typical Application

Figure 4-1 shows a typical configuration for a transceiver built with the chip set. This section presents some example filters, diagrams, and component values for reference.

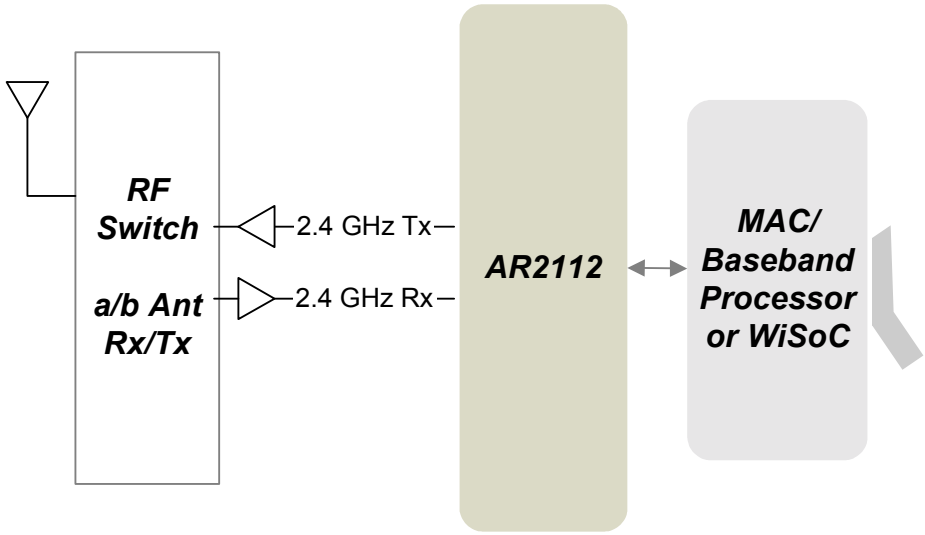


Figure 4-1. **Typical Application Block Diagram using the AR2112**

5. Package Dimensions

The AR2112 is packaged in a JEDEC MO-220 compliant leadless plastic chip carrier (LPCC). The LPCC can be sourced from any one of three package drawings. The external dimensions are identical from all sources.

The LPCC package drawings and dimensions are provided in Figure 5-1, Figure 5-2, and Figure 5-3, and in Table 5-1.

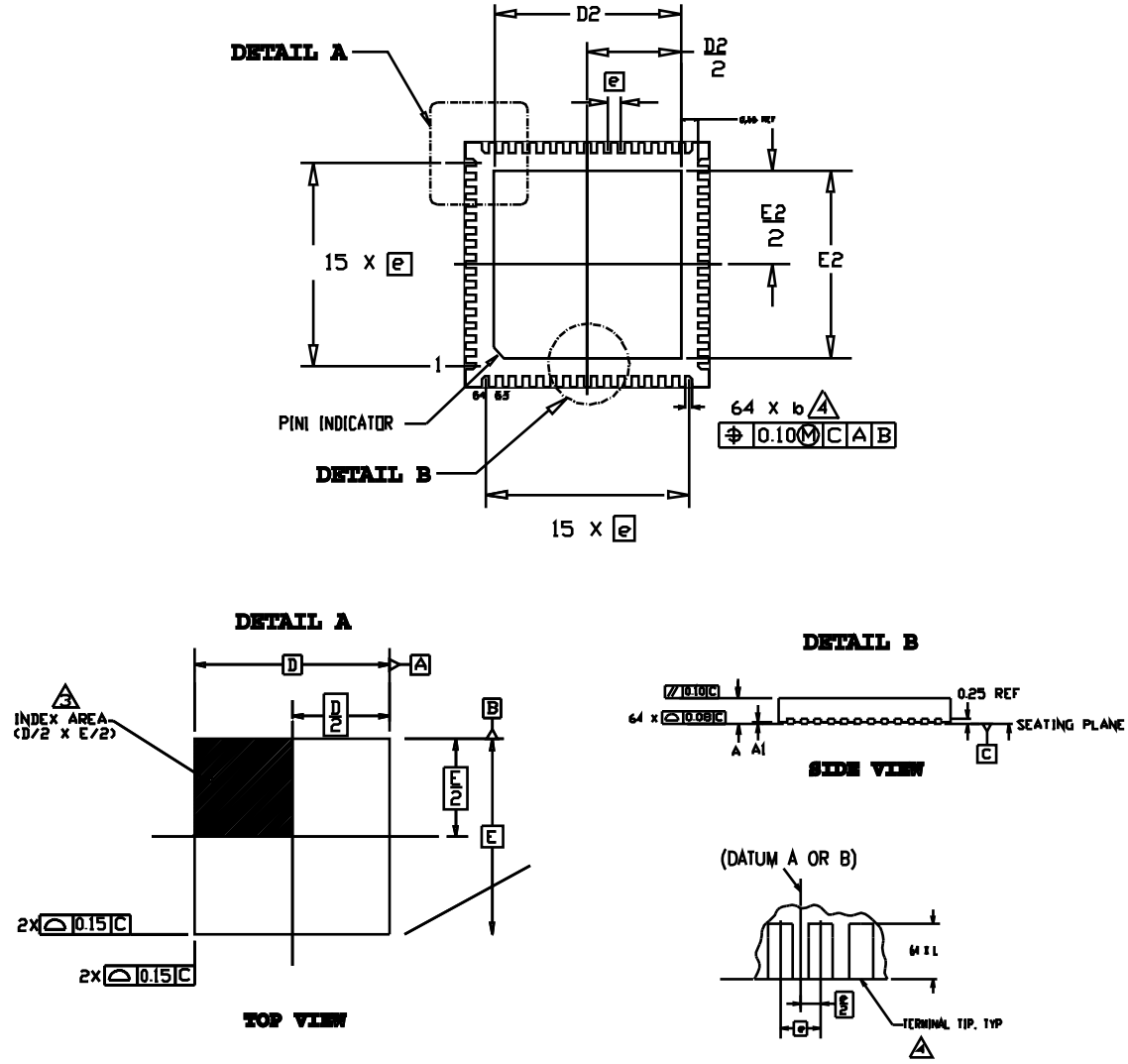


Figure 5-1. **AR2112 "Package A" Dimensions**

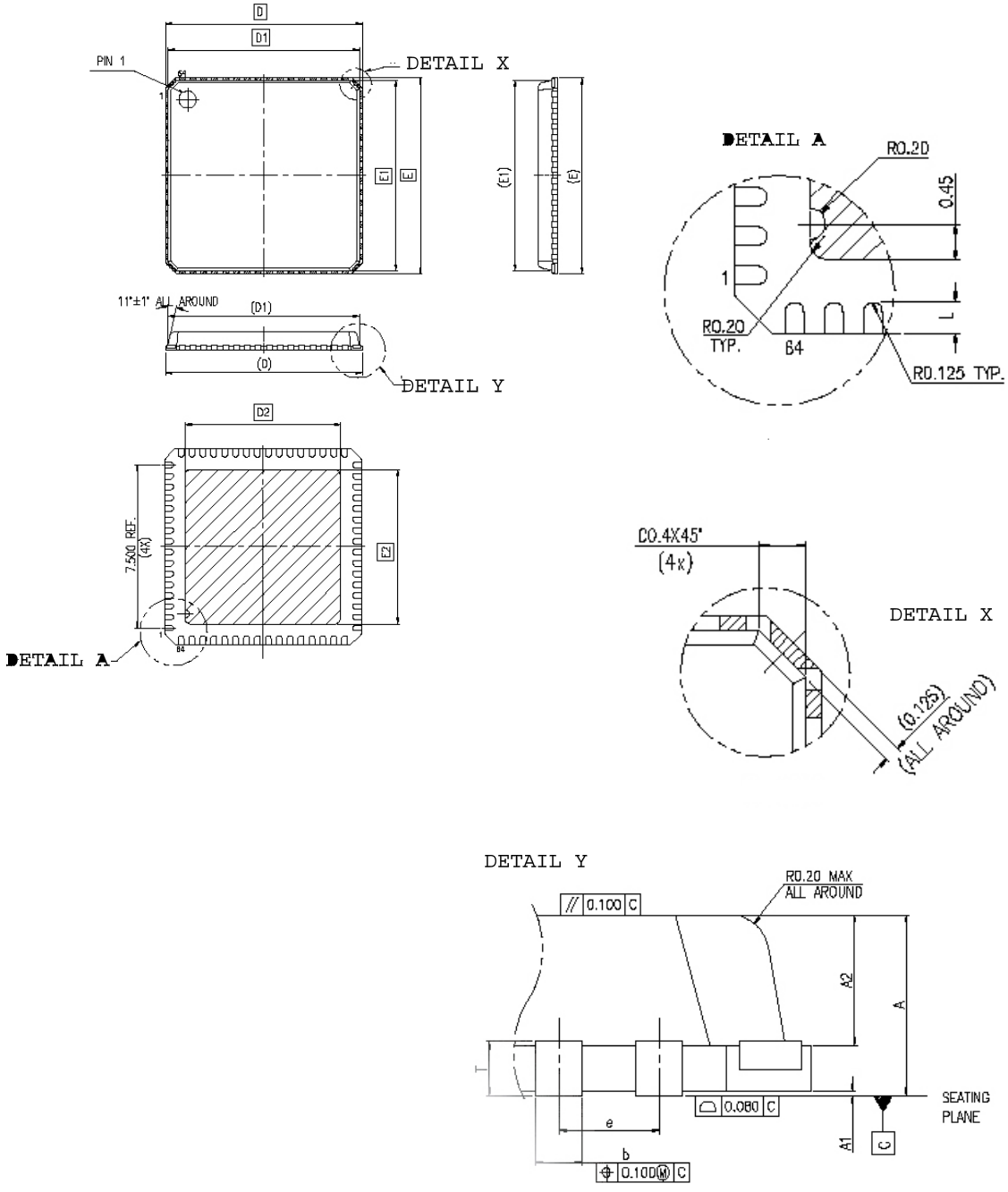


Figure 5-2. **AR2112 "Package B" Dimensions**

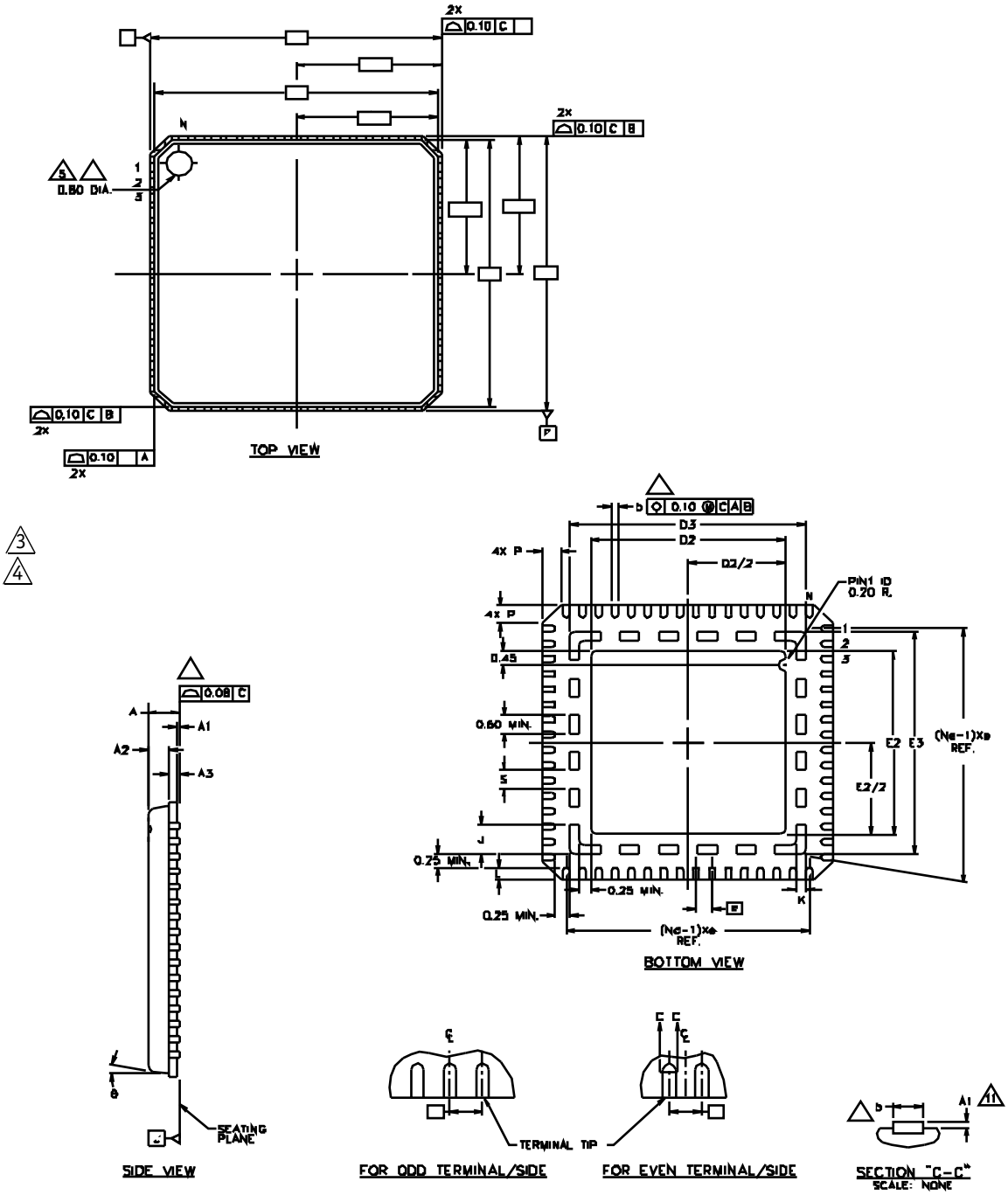


Figure 5-3. **AR2112 "Package C" Dimensions**

Table 5-1. **LPCC "Package A, B, and C" Dimensions**

Dimension Label	Min.	Nom.	Max.	Unit.	Description
A	0.80	0.90	1.00	mm	Thickness
A1	0	0.02	0.05	mm	Standoff
A2	0.60	0.65	0.70	mm	Cavity Thickness (Package B only)
A3		0.20		mm	
b	0.23	0.25	0.28	mm	Lead Width
D	8.90	9.00	9.10	mm	Package Length
D1	8.65	8.75	8.85	mm	Cavity Length (Package B only)
D2	6.75	6.90	7.05	mm	Exposed PAD Length
D3	7.15	7.30	7.45	mm	
E	8.90	9.00	9.10	mm	Package Width
E1	8.65	8.75	8.85	mm	Cavity Width (Package B only)
E2	6.75	6.90	7.05	mm	Exposed PAD Width
E3	7.15	7.30	7.45	mm	
e		0.50 BSC.		mm	Lead Pitch
L	0.30	0.40	0.50	mm	Lead Length
JEDEC REF		MO-220			

Notes:

1 Dimensioning and tolerancing conform to ASME Y14-1994.
2 All dimensions are in millimeters, and all angles are in degrees.
3 The Terminal #1 identifier and terminal numbering convention shall conform to JESD 95-1 and SPP-012. Terminal #1 identifier L is located within the zone indicated. It may be either a mold or a marked feature.
4 Dimension b applies to metallized terminal and is measured from the terminal tip.

Ordering Information

The order number is determined by the selection of these options. See the following example.

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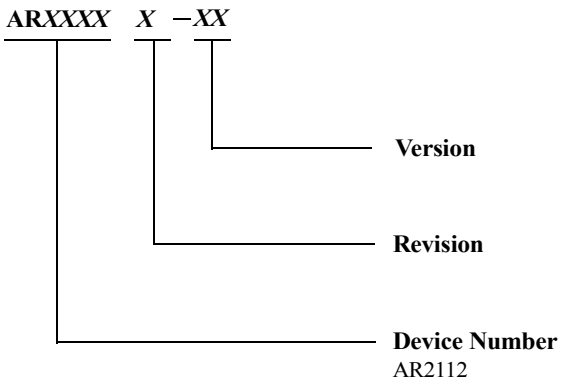

An order number, AR2112A-*00* specifies a current version of the AR2112.

Revision History

Revision	Description of Changes
April 2003	Initial draft
June 2003	Updated Electrical Characteristics.
September 2003	Updated Electrical Characteristics.
October 2003	Added “Package B” and updated Table 5-1, “LPCC ‘Package A and B’ Dimensions”.
March 2004	Upadated Package ‘A, B, and C’ Dimensions. Updated tcase temperature.

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