AR2316 Single Chip MAC/Baseband/Radio and Processor for 2.4 GHz Wireless LANs

General Description

The Atheros AR2316 integrated the MAC/baseband/radio and processor into a single chip for wireless access point and router applications. It includes a 2.4 GHz radio, MIPS 4000 processor, 802.11 MAC/baseband processor, 802.3 Ethernet MAC and MII interface, SDRAM controller, external memory interface for Flash, ROM, or RAM, PCI bus interface or a flexible local bus, UART, GPIOs, LED controls.

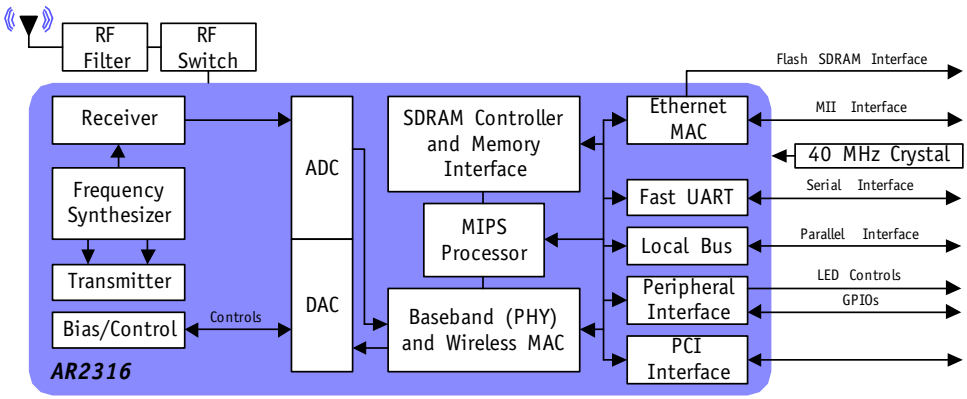
The AR2316 implements an 802.11 MAC/baseband processor supporting all IEEE 802.11g data rates (1 to 54 Mbps) and all IEEE 802.11b complementary key coding (CCK) data rates (1 to 11 Mbps). In Atheros Super G™ mode, AR2316 supports data rates up to 108 Mbps. Additional features include forward error correction coding at rates for 1/2, 2/3, and 3/4, signal detection, automatic gain control, frequency offset estimation, symbol timing, channel estimation, error recovery, enhanced security, and quality of service (QoS). The AR2316 performs receive and transmit filtering for IEEE 802.3 and 802.11 networks.

The AR2316 is an all CMOS, highly integrated single-chip solution that supports 802.11b/g WLANs.

Features

- Integrated MIPS 4000 processor
- 180 MHz processor frequency
- IEEE 802.11b/g Access Point, Ad Hoc, and station functions supported
- OFDM and CCK modulation schemes supported
- Data rates of 1, 2, 5.5, 6, 9, 11, 12, 18, 24, 36, 48, 54 Mbps and Atheros Super G™ mode offering up to 108 Mbps
- IEEE 802.3 Ethernet MAC supporting 10/100 Mbps, full and half duplex, and MII interface to external Ethernet PHY
- UART for console support
- Flexible, programmable local bus
- PCI bus host and client modes
- IEEE 1149.1 standard test access port and boundary scan architecture supported
- EJTAG based debugging of the processor core supported
- Standard 0.18 µm CMOS technology
- 15 mm x 15 mm 233 PBGA package

System Block Diagram



1. Pin Descriptions

This section contains both a package pinout (see Table 1-1 through Table 1-4) and tabular listings of the signal descriptions.

The following nomenclature is used for signal names:

- NC indicates no connection should be made to this pin.
- _L at the end of the signal name indicates active low signal.
- P at the end of the signal name indicates the positive side of a differential signal.
- N at the end of the signal name indicates the negative side of a differential signal.

The following nomenclature is used for signal types:

- IA indicates an analog input signal.
- I indicates a digital input signal.
- IH indicates input signals with weak internal pull-up, to prevent signals from floating when left open.
- IL indicates input signals with weak internal pull-down, to prevent signals from floating when left open.
- I/O indicates a digital bidirectional signal.
- OA indicates an analog output signal.
- O indicates a digital output signal.
- P indicates a power or ground signal.

Table 1-1. **AR2316 Pin Assignments (1–9) [1]**

	1	2	3	4	5	6	7	8	9
A	GPIO_7	PCI_CBE1_L / LB_WE_L	GPIO_5	GPIO_3	GPIO_2	GPIO_1	MODE_SEL_1	WF_ANTC	WF_ANTB
B	GPIO_6	PCI_AD_14 / LB_ADDR_13	PCI_DEVSEL_L / LB_ADDR_2	GPIO_4	PCI_SERR_L / LB_DATA_1	PCI_CLKRUN_L / LB_DATA_5	WF_ANTD	PCI_AD_16 / LB_ADDR_15	WF_ANTA
C	PCI_AD_15 LB_ADDR_14	PROC_REF_CLK	GND	PCI_PERR_L / LB_DATA_0	GPIO_0	MODE_SEL_0	PCI_FRAME_L / LB_WAIT_L	PCI_IRDY_L / LB_ADDR_0	PCI_CBE2_L / LB_OE_L
D	PCI_AD_11 / LB_ADDR_10	PCI_AD_12 / LB_ADDR_11	PCI_AD_13 / LB_ADDR_12	GND	PCI_STOP_L / LB_ADDR_1	PCI_TRDY_L / LB_INTR	VDD33	VDD33	VDD19
E	SD_DATA_1	SD_DATA_0	SD_DATA_15	PCI_AD_10 / LB_ADDR_9	NA	NA	NA	NA	NA
F	SD_DATA_14	PCI_AD_9 / LB_DATA_15	SD_DATA_13	SD_DATA_2	NA	NA	NA	NA	NA
G	PCI_AD_8 / LB_DATA_14	SD_DATA_12	SD_DATA_8	SD_DATA_3	NA	NA	GND	GND	GND
H	SD_DATA_11	PCI_CBE0_L / LB_ADDR_5	VDD19	VDD19	NA	NA	GND	GND	GND
J	SD_DATA_10	PCI_AD_7 / LB_DATA_13	SD_WE_L	VDD19	NA	NA	GND	GND	GND
K	SD_DATA_9	PCI_AD_6 / LB_DATA_12	SD_DATA_4	VDD33	NA	NA	GND	GND	GND
L	PCI_AD_5 / LB_DATA_11	SD_DATA_5	PCI_AD_4 / LB_DATA_10	VDD33	NA	NA	GND	GND	GND
M	SD_DATA_6	SD_CAS_L	SD_DATA_7	SD_DQM_0	NA	NA	NA	NA	NA
N	PCI_AD_2 / LB_DATA_8	SD_DQM_1	PCI_AD_3 / LB_DATA_9	SD_RAS_L	NA	NA	NA	NA	NA
P	SD_CLK	PCI_AD_0 / LB_DATA_6	SD_CLK_FB	GND	SD_BANK_0	PCI_REQ1_L / LB_ADDR_7	SD_ADDR_1	VDD19	VDD19
R	SD_BANK_1	SD_CKE	GND	SD_ADDR_9	SD_ADDR_8	SD_ADDR_6	SD_ADDR_12	PCI_GNT1_L / LB_ADDR_8	ETH_CRS
T	PCI_AD_1 / LB_DATA_7	SD_CS_L	PCI_INT_L / LB_DATA_4	SD_ADDR_0	PCI_GNT0_L / LB_DATA_3	SD_ADDR_2	SD_ADDR_5	PCI_AD_29 / GPIO_20	PCI_AD_30 / GPIO_21
U	SD_ADDR_10	SD_ADDR_11	PCI_RST_L / LB_CS	PCI_REQ0_L / LB_DATA_2	SD_ADDR_7	PCI_AD_31 / GPIO_22	SD_ADDR_4	SD_ADDR_3	ETH_TXD_3

[1]Note that two listed pin assignments show multiplexing pins, and list the PCI pin name / Local Bus / GPIO pin name.

Table 1-2. **AR2316 Pin Assignments (10–17) [1]**

	10	11	12	13	14	15	16	17
A	RFOUTN_BIAS	RFOUTN	RFOUTP	RFOUTP_BIAS	AGND	RFINN	RFINP	AGND
B	AGND	AVDD	AVDD	AGND	AGND	AGND	AGND	AGND
C	AVDD	PDETN	PDETP	AVDD33	NC	AGND	NC	NC
D	VDD19	PCI_EPRM_EN_L	AVDD	AVDD33	AGND	AVDD	NC	NC
E	NA	NA	NA	NA	AVDD33	BIASREF	AGND	AVDD
F	NA	NA	NA	NA	AVDD33	VREG_OUT	NC	NC
G	GND	GND	NA	NA	VDD33	AGND	AVDD	AVDD33
H	GND	GND	NA	NA	VDD33	VREG_COMP	XTALO	XTALI
J	GND	GND	NA	NA	VDD19	UART_SIN	PCI_AD_18 / GPIO_9	UART_SOUT
K	GND	GND	NA	NA	VDD19	TRST_L	PCI_AD_17 / GPIO_8	EJTAG_SEL
L	GND	GND	NA	NA	PCI_PAR / LB_RDY_L	TCLK	TDI	TDO
M	NA	NA	NA	NA	SPI_MOSI	PCI_AD_20 / GPIO_11	COLD_RST_L	TMS
N	NA	NA	NA	NA	ETH_RXC	SPI_CS_L	SPI_CK	PCI_AD_19 / GPIO_10
P	VDD33	VDD33	ETH_TXD_0	PCI_CBE3_L / LB_ADDR_6	GND	ETH_MDIO	SPI_MISO	PCI_AD_22 / GPIO_13
R	VDD33	ETH_TXD_1	ETH_COL	ETH_RXD_0	ETH_RXD_1	GND	PCI_CLK / LB_ADDR_4	ETH_RESET_L
T	ETH_TXD_2	PCI_AD_28 / GPIO_19	ETH_RXERR	PCI_AD_26 / GPIO_17	PCI_AD_24 / GPIO_15	ETH_TXC	PCI_IDSEL / LB_ADDR_3	PCI_AD_21 / GPIO_12
U	PCI_AD_27 / GPIO_18	PCI_AD_25 / GPIO_16	ETH_RXDV	ETH_TXEN	ETH_RXD_2	ETH_RXD_3	PCI_AD_23 / GPIO_14	ETH_MDC

[1]Note that two listed pin assignments show multiplexing pins, and list the PCI pin name / Local Bus / GPIO pin name.

Table 1-3 and Table 1-4 provide the signal-to-pin relationship information for the AR2316.

Table 1-3. **PCI Signal to Pin Relationships and Descriptions**

Signal Name	Pin	Direction	Description
PCI_CLK	R16	I/O	PCI clock, input for target, output for master
PCI_AD_31	U6[1]	I/O	Multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contains a physical byte address. During subsequent clocks, it contains data.
PCI_AD_30	T9[1]	I/O	
PCI_AD_29	T8[1]	I/O	
PCI_AD_28	T11[1]	I/O	
PCI_AD_27	U10[1]	I/O	
PCI_AD_26	T13[1]	I/O	
PCI_AD_25	U11[1]	I/O	
PCI_AD_24	T14[1]	I/O	
PCI_AD_23	U16[1]	I/O	
PCI_AD_22	P17[1]	I/O	
PCI_AD_21	T17[1]	I/O	
PCI_AD_20	M15[1]	I/O	
PCI_AD_19	N17[1]	I/O	
PCI_AD_18	J16[1]	I/O	
PCI_AD_17	K16[1]	I/O	
PCI_AD_16	B8[1]	I/O	
PCI_AD_15	C1[1]	I/O	
PCI_AD_14	B2[1]	I/O	
PCI_AD_13	D3[1]	I/O	
PCI_AD_12	D2[1]	I/O	
PCI_AD_11	D1	I/O	
PCI_AD_10	E4	I/O	
PCI_AD_9	F2	I/O	
PCI_AD_8	G1[1]	I/O	
PCI_AD_7	J2[1]	I/O	
PCI_AD_6	K2[1]	I/O	
PCI_AD_5	L1[1]	I/O	
PCI_AD_4	L3[1]	I/O	
PCI_AD_3	N3[1]	I/O	
PCI_AD_2	N1[1]	I/O	
PCI_AD_1	T1[1]	I/O	
PCI_AD_0	P2[1]	I/O	
PCI_CBE3_L	P13	I/O	PCI multiplexed bus command and byte enables. During the address phase of a transaction, these signals define the bus command. During the data phase, they are used as byte enables.
PCI_CBE2_L	C9[1]	I/O	
PCI_CBE1_L	A2[1]	I/O	
PCI_CBE0_L	H2	I/O	
PCI_CLKRUN_L	B6[1]	I	Provides for starting and stopping the PCI clock.
PCI_DEVSEL_L	B3[1]	I/O	PCI device select.
PCI_EPRM_EN_L	D11	I	PCI EEPROM enable
PCI_FRAME_L	C7[1]	I/O	PCI frame.
PCI_GNT1_L	R8[1]	I	PCI grant.
PCI_GNT0_L	T5[1]	I	
PCI_IDSEL	T16[1]	I	PCI ID select.

Table 1-3. **PCI Signal to Pin Relationships and Descriptions**

Signal Name	Pin	Direction	Description
PCI_INT_L	T3[1]	O	PCI interrupt.
PCI_IRDY_L	C8[1]	I/O	PCI initiator ready.
PCI_PAR	L14[1]	I/O	PCI parity.
PCI_PERR_L	C4[1]	I/O	PCI parity error.
PCI_REQ1_L	P6[1]	O	PCI request.
PCI_REQ0_L	U4[1]	O	
PCI_RST_L	U3[1]	I	PCI Reset
PCI_SERR_L	B5[1]	I/O	PCI system error.
PCI_STOP_L	D5[1]	I/O	PCI stop.
PCI_TRDY_L	D6[1]	I/O	PCI target ready.

[1]This pin is multiplexed. See Table 1-1 and Table 1-2 for more information.

Table 1-4. **Signal-to-Pin Relationships**

Signal Name	Pin	Direction	Description
General			
BIASREF	E15	IA	Connects a 6.19 Ω ±1% resistor to ground.
COLD_RST_L	M16	I	Reset entire chip
SPI_CK	N16		SPI Serial Flash Clock
SPI_CS_L	N15		SPI Serial Flash Chip Select
SPI_MISO	P16		SPI Serial Flash Data: Master In, Slave out
SPI_MOSI	M14		SPI Serial Flash Data: Master Out, Slave In
VREG_COMP	H15	OA	Compensation node for voltage regulator
VREG_OUT	F15	IA	1.9 V voltage regulator output
XTALI	H17	I	40 MHz crystal
XTALO	H16	O	40 MHz crystal
PROC_REF_CLK	C2	I	Processor reference clock
Local Bus			
LB_ADDR_0	C8[1]	I	Address[0]
LB_ADDR_1	D5[1]	I	Address[1]
LB_ADDR_2	B3[1]	I	Address[2]
LB_ADDR_3	T16[1]	I	Address[3]
LB_ADDR_4	R16[1]	I	Address[4]
LB_ADDR_5	H2[1]	I	Address[5]
LB_ADDR_6	P13[1]	I	Address[6]
LB_ADDR_7	P6[1]	I	Address[7]
LB_ADDR_8	R8[1]	I	Address[8]
LB_ADDR_9	E4[1]	I	Address[9]
LB_ADDR_10	D1[1]	I	Address[10]
LB_ADDR_11	D2[1]	I	Address[11]
LB_ADDR_12	D3[1]	I	Address[12]
LB_ADDR_13	B2[1]	I	Address[13]
LB_ADDR_14	C1[1]	I	Address[14]
LB_ADDR_15	B8[1]	I	Address[15]

Table 1-4. **Signal-to-Pin Relationships (continued)**

Signal Name	Pin	Direction	Description
LB_DATA_0	C4[1]	I/O	Data bus. For eight-bit reads, unselected parts of the bus are not driven.
LB_DATA_1	B5[1]	I/O	
LB_DATA_2	U4[1]	I/O	
LB_DATA_3	T5[1]	I/O	
LB_DATA_4	T3[1]	I/O	
LB_DATA_5	B6[1]	I/O	
LB_DATA_6	P2[1]	I/O	
LB_DATA_7	T1[1]	I/O	
LB_DATA_8	N1[1]	I/O	
LB_DATA_9	N3[1]	I/O	
LB_DATA_10	L3[1]	I/O	
LB_DATA_11	L1[1]	I/O	
LB_DATA_12	K2[1]	I/O	
LB_DATA_13	J2[1]	I/O	
LB_DATA_14	G1[1]	I/O	
LB_DATA_15	F2[1]	I/O	
LB_CS	U3[1]	I/O	Local bus chip select
LB_INTR	D6[1]	I/O	Local bus interrupt
LB_RDY_L	L14[1]	I/O	Local bus ready
LB_OE_L	C9[1]	I/O	Output enable
LB_WAIT_L	C7[1]	I/O	Asserted to keep the host from asserting LB_OE_L or LB_WE_L. On reads, used to wait for the read data to be valid. On writes, used to postpone new requests until the previous write finishes.
LB_WE_L	A2[1]	I/O	Write enable

Table 1-4. **Signal-to-Pin Relationships (continued)**

Signal Name	Pin	Direction	Description
GPIO			
GPIO_0	C5	I/O	General purpose GPIO pins
GPIO_1	A6	I/O	
GPIO_2	A5	I/O	
GPIO_3	A4	I/O	
GPIO_4	B4	I/O	
GPIO_5	A3	I/O	
GPIO_6	B1	I/O	
GPIO_7	A1	I/O	
GPIO_8	K16[1]	I/O	
GPIO_9	J16[1]	I/O	
GPIO_10	N17[1]	I/O	
GPIO_11	M15[1]	I/O	
GPIO_12	T17[1]	I/O	
GPIO_13	P17[1]	I/O	
GPIO_14	U16[1]	I/O	
GPIO_15	T14[1]	I/O	
GPIO_16	U11[1]	I/O	
GPIO_17	T13[1]	I/O	
GPIO_18	U10[1]	I/O	
GPIO_19	T11[1]	I/O	
GPIO_20	T8[1]	I/O	
GPIO_21	T9[1]	I/O	
GPIO_22	U6[1]	I/O	
Ethernet			
ETH_COL	R12	I	Collision Detect
ETH_CRS	R9	I	MII interface carrier sense
ETH_MDIO	P15	I/O	PHY chip control bus data
ETH_MDC	U17	O	PHY chip control bus clock
ETH_RESET_L	R17	O	PHY Reset
ETH_RXC	N14	I	Receive Clock (2.5 MHz @ 10 Mb; 25 MHz @ 100 Mb)
ETH_RXD_0	R13	I	Receive Data
ETH_RXD_1	R14	I	
ETH_RXD_2	U14	I	
ETH_RXD_3	U15	I	
ETH_RXDV	U12	I	Receive Data Valid
ETH_RXERR	T12	I	Receive Error
ETH_TXC	T15	I	Transmit Clock (2.5MHz @ 10Mbit; 25MHz @ 100Mbit)
ETH_TXD_0	P12	O	Transmit Data
ETH_TXD_1	R11	O	
ETH_TXD_2	T10	O	
ETH_TXD_3	U9	O	
ETH_TXEN	U13	O	Transmit Enable
JTAG Interface			
EJTAG_SEL	K17	I	When asserted, JTAG pins are routed to EJATAG TAP controller. When deasserted, JTAG pins are routed to TAP controller.
TCLK	L15	I	JTAG test clock
TDI	L16	I	JTAG data input

Table 1-4. **Signal-to-Pin Relationships (continued)**

Signal Name	Pin	Direction	Description
TDO	L17	O	JTAG data output
TMS	M17	I	JTAG test mode
TRST_L	K15	I	JTAG test reset
Mode Selection			
MODE_SEL_1	A7	I	Selects the desired bus configuration
MODE_SEL_0	C6	I	■ 00 = PCI client mode ■ 01 = Local bus ■ 10 = Reserved ■ 11 = PCI host mode If left open, the bus configuration is PCI client mode.
RF Interface			
PDETN	C11	IA	Differential Power detector
PDETP	C12	IA	
RFINN	A15	IA	Differential RF input
RFINP	A16	IA	
RFOUTN	A11	OA	Differential RF output
RFOUTP	A12	OA	
RFOUTP_BIAS	A13	IA	1.9 V
RFOUTN_BIAS	A10	IA	1.9 V
Antenna Control			
WF1_ANTA	B9	O	Antenna selection
WF1_ANTB	A9	O	
WF1_ANTC	A8	O	
WF1_ANTD	B7	O	
DRAM Control			
SD_DATA_15	E3	I/O	Read/write data [15]
SD_DATA_14	F1	I/O	Read/write data [14]
SD_DATA_13	F3	I/O	Read/write data [13]
SD_DATA_12	G2	I/O	Read/write data [12]
SD_DATA_11	H1	I/O	Read/write data [11]
SD_DATA_10	J1	I/O	Read/write data [10]
SD_DATA_9	K1	I/O	Read/write data [9]
SD_DATA_8	G3	I/O	Read/write data [8]
SD_DATA_7	M3	I/O	Read/write data [7]
SD_DATA_6	M1	I/O	Read/write data [6]
SD_DATA_5	L2	I/O	Read/write data [5]
SD_DATA_4	K3	I/O	Read/write data [4]
SD_DATA_3	G4	I/O	Read/write data [3]
SD_DATA_2	F4	I/O	Read/write data [2]
SD_DATA_1	E1	I/O	Read/write data [1]
SD_DATA_0	E2	I/O	Read/write data [0]
SD_CLK	P1	O	SDRAM clock
SD_CKE	R2	O	SDRAM clock enable
SD_CLK_FB	P3	I	SDRAM clock feedback
SD_CAS_L	M2	O	Column address select
SD_RAS_L	N4	O	Row address select
SD_CS_L	T2	O	Chip select for DRAM
SD_BANK_1	R1	O	Bank address [1]
SD_BANK_0	P5	O	Bank address [0]
SD_DQM_1	N2	O	Data mask for byte 1
SD_DQM_0	M4	O	Data mask for byte 0
SD_WE_L	J3	O	Write enable

Table 1-4. **Signal-to-Pin Relationships (continued)**

Signal Name	Pin	Direction	Description
SD_ADDR_12	R7	O	Row/column address within bank
SD_ADDR_11	U2	O	
SD_ADDR_10	U1	O	
SD_ADDR_9	R4	O	
SD_ADDR_8	R5	O	
SD_ADDR_7	U5	O	
SD_ADDR_6	R6	O	
SD_ADDR_5	T7	O	
SD_ADDR_4	U7	O	
SD_ADDR_3	U8	O	
SD_ADDR_2	T6	O	
SD_ADDR_1	P7	O	
SD_ADDR_0	T4	O	
UART Control			
UART_SOUT	J17	O	Serial output data
UART_SIN	J15	I	Serial input data
Power			
AGND	A14, A17, B10, B13, B14, B15, B16, B17, C15, D14, E16, G15		Analog ground
AVDD	B11, B12, C10, D12, D15, E17, G16		Analog 1.9V supply
AVDD33	C13, D13, E14, F14, G17		Analog 3.3V supply
NA	E5, E6, E7, E8, E9, E10, E11, E12, E13, F5, F6, F7, F8, F9, F10, F11, F12, F13, G5, G6, G12, G13, H5, H6, H12, H13, J5, J6, J12, J13, K5, K6, K12, K13, L5, L6, L12, L13, M5, M6, M7, M8, M9, M10, M11, M12, M13, N5, N6, N7, N8, N9, N10, N11, N12, N13		Not Applicable
GND	C3, D4, G7, G8, G9, G10, G11, H7, H8, H9, H10, H11, J7, J8, J9, J10, J11, K7, K8, K9, K10, K11, L7, L8, L9, L10, L11, P4, P14, R3, R15		Digital ground
VDD19	D9, D10, H3, H4, J4, J14, K14, P8, P9		Digital 1.9V
VDD33	D7, D8, G14, H14, K4, L4, P10, P11, R10		Digital 3.3V
No Connection			
NC	C14, C16, C17, D16, D17, F16, F17		No connection, must be open

[1]This pin is multiplexed. See Table 1-1 and Table 1-2 for more information.

Document Number: 981-00030-001 MKG-0258 Rev. 1

Atheros Communications Incorporated
529 Almanor Avenue
Sunnyvale, CA 94086
t: 408/773-5200
f: 408/773-9940
www.atheros.com