A Highly Integrated Analog Front-End for 3G

Waleed Khalil, Tsung-Yuan Chang, Xuewen Jiang, Syed R. Naqvi, Babak Nikjou, and James Tseng

***Abstract*—This paper describes a reconfigurable analog front-end (AFE) and audio Codec IC supporting the wideband code division multiple access (WCDMA) standard. The chip is fabricated on Intel's 0.18-μm (SOC) flash + logic + analog (FLA) process technology using a 0.35-μm feature size analog transistor. The transmit path contains a 10-bit segmented rail-to-rail digital-to-analog converter, automatically tunable active *RC* filter, and programmable gain amplifier (PGA) with self-tuning gain and offset correction circuit. The receive path incorporates a PGA, active *RC* filter, and an 8-bit analog-to-digital converter with built-in offset correction. The AFE operates at 2.7 V with a current consumption of 55 mA and total active area of 15 mm^2.**

***Index Terms*—Active *RC* filter, analog baseband, analog front-end (AFE), programmable gain amplifier (PGA), wireless transmitters and receivers.**

I. Introduction

WIDEBAND code division multiple access (WCDMA) is predicted to become the most dominant standard when the cellphone industry transitions from voice to high-datarate-based applications such as video transmission and interactive video games. In comparison with a GSM system that uses 200-kHz channel spacing, WCDMA uses 5-MHz channel spacing and is, therefore, able to achieve a maximum data rate of 2 Mb/s. In order to adjust to this order of magnitude increase in bandwidth from GSM to WCDMA, a new architecture is developed for the analog front-end (AFE) [1].

Combining analog and digital baseband along with Flash and SRAM memory on a single die provides the ultimate integration for a cellular system-on-chip (SOC). Although this integration achieves the best performance and lowest power/area, it results in a noisy environment that is hostile to analog circuits. In addition, previous attempts to achieve this level of integration resulted in sacrificing the performance of the analog and/or digital transistor. This paper describes a reconfigurable AFE fabricated on Intel's advanced flash + logic + analog (FLA) process technology. This AFE integration with digital and flash achieves die-area and power savings unattainable by using multicomponent chipsets.

This paper covers the major blocks in the WCDMA AFE transceiver, with major focus on the transmit side. The organization of this paper is as follows. Section II presents an overall review of the chip architecture. Section III details the transmitter part of the AFE, including the digital-to-analog converter (D/A), filter, and programmable gain amplifier (PGA). Section IV discusses the receiver part of the AFE. The layout and experimental results are presented in Section V. Finally, in Section VI, the paper concludes with a summary.

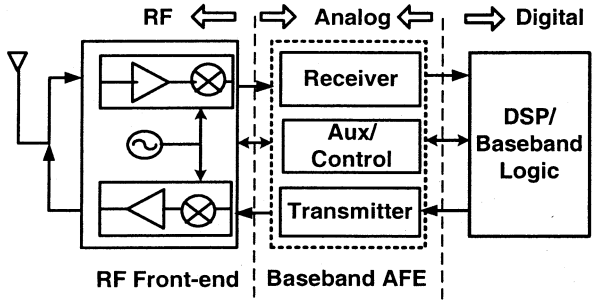


Fig. 1. Typical wireless system.

II. AFE Architecture

Fig. 1 illustrates a typical wireless system, where three distinct sections are shown. The RF front-end section is responsible for amplification as well as downconverting/upconverting of the RF signal to/from low-frequency baseband signal. The baseband AFE processes the signal in the low-frequency domain. In the receiver part of the AFE (also known as the demodulator), the small signal is further gained and filtered, then digitized using an analog-to-digital coonverter (A/D). The AFE transmitter (known as the modulator) is responsible for converting digitally modulated symbols into an analog signal using a D/A, followed by filtering and gain stages. The auxiliary section is mainly responsible for controlling the RF system as well as general phone functions. Last is the digital baseband module, which is used for the main digital modulation and demodulation/detection functions. A detailed description of the specifications for the WCDMA system is available on the 3GPP website.[1]

A block diagram detailing the architecture of the AFE is shown in Fig. 2, where the main channels are the transmit channel, receive channel, and auxiliary channel. In the transmit channel, 10-bit digitally modulated data is received from the digital section of baseband modem by the I–Q D/A. The architecture of the 10-bit D/A is based on a fully differential segmented voltage mode R-2R, reported for the first time at the high sampling rate of 15.36 MHz. The R-2R architecture utilizes a ladder network of R-2R resistors to obtain binary weighted voltages. Following the D/A is the transmitter (TX) filter, which limits the bandwidth of the signal to the channel bandwidth and reduces any spurious emission caused by the D/A glitch energy. The TX filter is a fifth-order Butterworth active *RC* filter with power-on self-calibration. The filter relies on a 4-bit capacitor trimming approach to achieve $+/-$ 7% bandwidth accuracy, while achieving a passband gain flatness

Manuscript received August 2, 2002; revised December 18, 2002.

The authors are with Intel Corporation, Chandler, AZ 85226 USA (e-mail: waleed.khalil@intel.com).

Digital Object Identifier 10.1109/JSSC.2003.810059

[1][Online.] Available: http://www.3gpp.org/specs/specs.htm

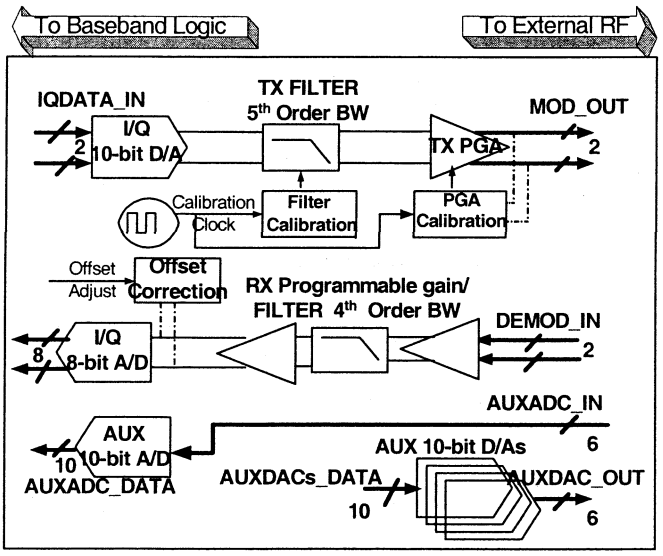


Fig. 2. AFE block diagram.

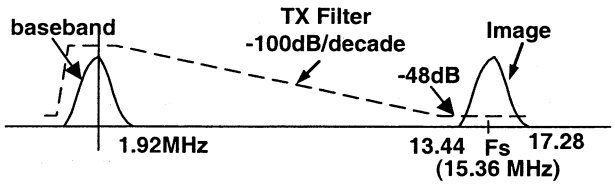


Fig. 3. Frequency spectrum of the transmit signal with the filter rolloff superimposed.

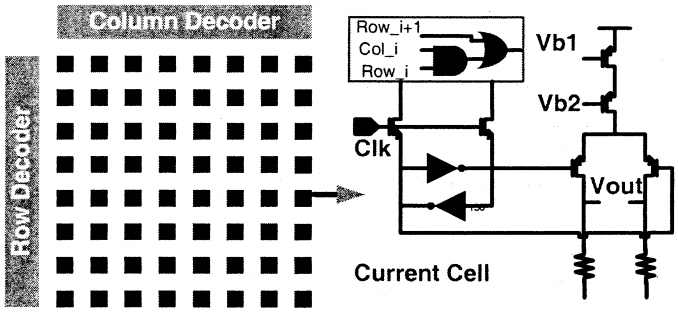


Fig. 4. General architecture and circuit of the I-mode D/A.

of ≤ 0.20 dB and total harmonic distortion (THD) ≤ -70 dB. Following the filter, a five-level PGA is used to adjust the output signal level and automatically calibrate the channel offset error upon the transmitter power-on or system request.

In the receive path, an input buffer is used in the first stage to perform two important functions: as a high-pass filter for dc offset blocking, and to improve the third-order input intercept point (IIP3) of the receiver through reducing the inter-modulation distortion (IMD) level. Following the buffer is a combination of a fourth-order Butterworth active *RC* filter and PGA. Finally, an 8-bit 15.36-MS/s A/D is used along with built-in multibit D/A for channel offset correction. The output data of the A/D is consequently latched and sent to the digital baseband modem

The auxiliary path includes a 10-bit cyclic A/D used for control purposes (e.g., battery testing) along with six R-string D/As for RF control functions. A 4-bit serial bus is used as the digital interface for the chip to control both the AFE and the audio Codec.

III. Transmitter Design

The requirements for a transmitter are dictated by the desired bit error rate (BER) and the adjacent channel power ratio (ACPR) after digital filtering in the baseband. The transmitter has two symmetrical channels, namely, in-phase (I channel) and quadrature (Q channel). The transmit signal generated by the baseband processor is a hybrid phase shift keying (HPSK) modulated digital signal with a bandwidth of 1.92 MHz. This 1.92-MHz digital signal is $4\times$ oversampled by the D/A at a sampling frequency of 15.36 MHz. The transmit frequency mask primarily dictates the filter transition band and stop-band profile in order to minimize spurious emissions and adjacent channel leakage. Additionally, the image attenuation requirement at the sampling frequency is another key factor for the filter rolloff. With a five-pole Butterworth filter, a 100-dB/decade rolloff is achieved, ensuring a 48-dB attenuation of the image that appears between 13.44–17.28 MHz, as shown in Fig. 3.

A. TX-IQ D/A

The I–Q D/A is the major building block that converts the binary-weighted digital input signal to a proportional analog voltage level. The goal of the D/A reported here is to obtain intrinsic 9-bit accuracy for sampling speeds up to 15.36 MS/s. There are several factors that are usually considered during the D/A design process. The D/A resolution, clock rate, and spectral purity, as well as area and power efficiency, are key parameters that ultimately affect the overall system performance. First, a review of the I-mode D/A (the most common D/A architecture) will be presented. Then, a detailed discussion of the selected R-2R D/A will follow.

Current-steering (I-mode) D/As are typically the architecture of choice for medium- to high-speed applications [2]. I-mode D/As are based on an array of matched current cells organized in unary or binary weighted elements that are steered to the D/A output depending on the digital input code, as shown in Fig. 4. Architecture variants include two-stage, interpolated, and segmented current-steering architectures. The segmented architecture is the most frequently used to combine high conversion rate and high resolution. In this architecture, the least significant bits (LSBs) steer binary weighted current sources, while the most significant bits (MSBs) are thermometer encoded and steer a unary current source array. Special biasing techniques and switching sequence optimization are often used in these architectures to spatially average away the systematic and random threshold voltage mismatch of the current cells [3]. Since the I-mode D/A uses active devices only, it is compatible with digital CMOS processes and is inherently a high-speed architecture. However, this architecture has some limitations in terms of power and area efficiency for the targeted speed and required resolution. Since reducing the cell current leads to lower transistor overdrive voltage, the effect of threshold voltage $V_{\rm th}$ mismatch is magnified. This limits the raw resolution (without trimming/calibration) of the I-mode D/A to around eight bits. In order to get around this problem, the transistor size in the current

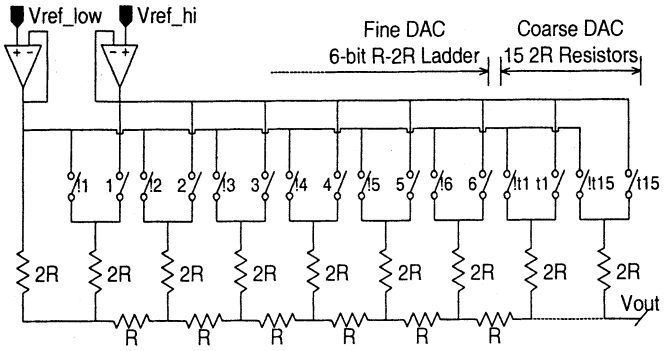


Fig. 5. Block diagram of the 10-bit segmented R-2R D/A.

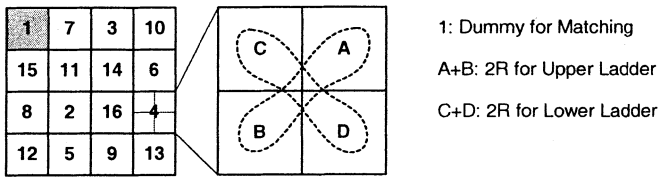


Fig. 6. Random walk technique for the segmented R-2R ladder.

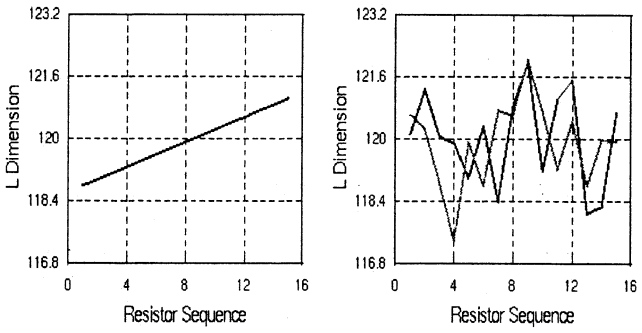


Fig. 7. A plot of resistor length versus resistor sequence (1–15 2Rs): (a) $\pm 1\%$ linear L mismatch. (b) $\pm 2\%$ random L mismatch.

cell (area and channel length) is increased, hence, increasing the transistor overdrive voltage while decreasing the effect of $V_{\rm th}$ mismatch. Although this helps in reducing the effect of $V_{\rm th}$ mismatch, it translates to excessive growth in area and capacitance, which limits the switching speed. Another solution to this problem is to increase the cell current, but this leads to higher power dissipation. Therefore, sacrificing either area or power is seen to be the fundamental limitation of the I-mode D/A.

A very popular architecture for the D/A uses R-2R ladders [4]. These ladders are used to realize binary weighted currents or voltages with a small number of components using a resistance ratio of only $2:1$, independent of the number of bits of resolution. The R-2R approach is compatible with both bipolar and CMOS technologies and is found to be highly efficient in resistor usage for D/As ranging from 6 to 16 bits. However, there are some disadvantages of the R-2R ladder architecture. In general, it requires good resistor matching to guarantee linearity and monotonicity. The switching transients at major code transitions also produce relatively large glitches. The proposed implementation uses segmentation and random walk techniques to realize a low-voltage, low-power, and area-efficient topology for an intrinsic 9-bit accuracy, without the need for trimming, calibration, tuning, or dynamic averaging.

In an R-2R ladder, it is necessary to have tight matching between each bit and the sum of all lesser bits in order to ensure monotonic operation. The segmented architecture allows this requirement to be relaxed and permits the construction of high-resolution converters. The block diagram of a 4/6 segmented 10-bit voltage division R-2R D/A is shown in Fig. 5, in which the coarse D/A consists of 2^4-1 identical resistors (1–15 2Rs), which are selected by a thermometer code. It is worth noting that for an R-2R ladder, the mismatch errors at the left end of the ladder are less significant than those at the right end (the segmented section). Consequently, large errors in the LSB resistors contribute proportionally less to the overall error than much smaller errors in the segmented resistors. Qualitatively, this is because the full-scale error due to a fractional error in an LSB is smaller than the same fractional error in an MSB. This observation indicates that more effort should be devoted to matching the segment resistors in the MSBs of the ladder than in the LSBs, since the former are more likely to determine the final accuracy than the latter.

In order to further reduce the sensitivity to resistor matching, a novel random-walk layout technique was utilized. This technique has been used very recently in a high-resolution current-steering D/A to realize 14-bit intrinsic accuracy [5]. The basic idea behind random walk is to average between positive differential nonlinearity (DNL) and negative DNL errors through hierarchical randomization. This technique (Fig. 6) improves the nonlinearity across process variations, since every 2R resistor for the same unary code is randomly placed to prevent first- and second-order systematic error residues from accumulating in the D/A output. In addition, mixing the upper and lower resistor ladders of the differential D/A helps in minimizing the differential offset error.

A simple Matlab program was used to demonstrate the strength of the random-walk layout technique. The simulation was done to compare between the D/A integral nonlinearity (INL) for $\pm 1\%$ linear dimension mismatch and those for $\pm 2\%$ random dimension mismatch in the segmented MSB portion. Fig. 7 shows a plot of the length of the resistors (L) versus the resistor sequence (1–15 2R segmented resistors) for the linear and random mismatch cases. The resistor width was kept the same for both cases. The random dimension mismatch data was generated using a normal distribution.

The INL analysis for $\pm 1\%$ linear mismatch and $\pm 2\%$ random mismatch is shown in Fig. 8. For the $\pm 1\%$ linear mismatch case, in which there is no spatial averaging effect, INL errors are accumulated as the digital input code increases. The maximum INL error is 2.5 LSB, which results in 8.5-bit accuracy for the 10-bit D/A. However, for the case of $\pm 2\%$ random mismatch, although the absolute mismatch magnitude is doubled compared to the linear case, the combined effect is a very desirable ± 1.2 LSB INL error, which results in a 9.8-bit accuracy for the 10-bit D/A. This is because the residual error above average and the residual error below average randomly compensate each other as the digital input code increases.

A principal challenge in designing a high-speed R-2R D/A is the voltage reference buffer design. The change of the equivalent

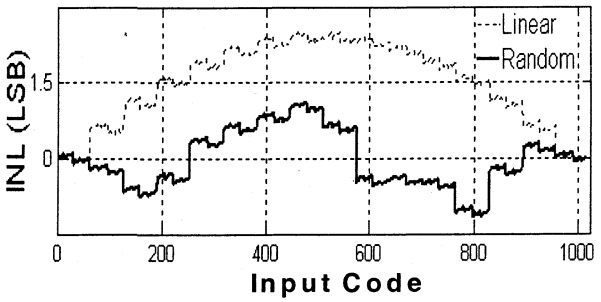


Fig. 8. INL for $\pm 1\%$ linear mismatch and $\pm 2\%$ random resistor mismatch.

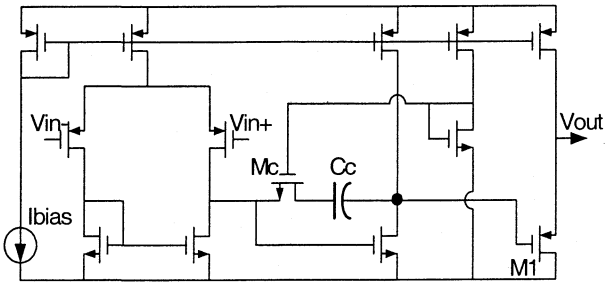


Fig. 9. Current sinking reference buffer ($V\mathrm{ref\_low}$).

resistance of an R-2R ladder for different input codes along with the need for high-speed simultaneous current sinking/sourcing dictates the need for a robust compensation scheme. Although class-AB amplifiers are widely used for this purpose, they have limited gain bandwidth (GBW), well below 50 MHz due to the builtin translinear loop stability of the output stage. After careful examination of the buffer requirement, it was realized that only a separate current sourcing or sinking capability is needed for each buffer. Thus, the $V\mathrm{ref\_hi}$ and $V\mathrm{ref\_low}$ buffers (Fig. 5) were realized separately using complementary architectures.

The buffer amplifier for the input voltage reference is designed with 50-MHz GBW, 65° phase margin (PM) , and $>$ 70 dB dc gain. The architecture employed is a two-stage amplifier with Miller and lead compensations. To drive the low resistive load of the D/A resistor network, a source follower stage is added, which makes the output impedance of the buffer as low as 100 Ω. For the differential design, a current sourcing capability is required for $V\mathrm{ref\_hi}$ while current sinking capability is required for $V\mathrm{ref\_low}$. A pMOS input stage and pMOS source follower is used for the current-sinking input buffer, as shown in Fig. 9, while a complementary nMOS input stage and nMOS source follower is used for the current-sourcing input buffer.

B. TX Filter

Several filter architectures were considered for the implementation of the transmit filter; such as gm-C filters, switch-cap filters (SCF) and active-*RC* filters. It is widely known that gm-C filters suffer from linearity limitation, which limits their THD well above -60 dB. For SCF, the rule of thumb is to design it using operational amplifiers (opamps) with GBW at least ten times wider than the sampling frequency. For WCDMA specification, this translates to opamps with GBW in excess of 153.6 MHz (ten times sampling rate),

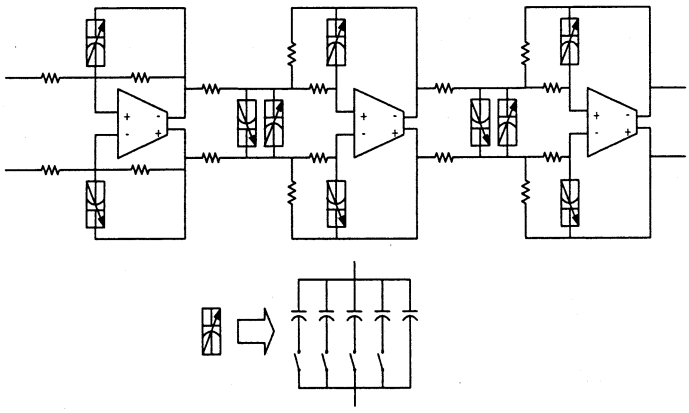


Fig. 10. Proposed fifth-order Butterworth filter.

which would consume a large amount of power. Furthermore, a continuous-time reconstruction filter is still needed after the SCF to remove the image at the sample rate. Thus, an active-*RC* filter with on-chip calibration circuit was chosen for its high linearity [6] and low power consumption.

The active-*RC* filter structure is shown in Fig. 10. The filter is connected directly to the R-2R D/A without the need for any additional buffer. To reduce the overall gain error when connecting the filter to the R-2R D/A, a first-order filter with the largest input resistance among all three stages is used as the filter input stage. Following that are two second-order biquad filters with multiple feedback network (MFB) [7]. The MFB structure uses only one opamp per biquad stage to minimize area and power consumption.

In order to adjust the filter cutoff frequency, either the resistors or the capacitors need to be programmable. It has been well documented [8] that parallel connected capacitor arrays have less area and better frequency range over parallel/series resistor or series capacitor arrays. In general, resistor-based tuning suffers from large distortion due to the variation of the switch resistance with the applied voltage. Increasing the switch size improves the distortion level but adds parasitic poles that shift the filter response and cause excessive ripple. Another reason to use capacitor tuning instead of resistor tuning in the proposed architecture is that capacitor arrays are less sensitive to the ON-switch resistance. This is because the ON-switch resistance is negligible to the C array impedance at the WCDMA baseband frequency range.

The parallel-connected capacitor array is realized by a fixed capacitance $C_{\min}$ and four binary-weighted switchable capacitors to provide a $+/-7\%$ tuning accuracy. The smallest switchable capacitance is denoted as C_{Δ}. The total value of the capacitor array C_{total} for any tuning code k is given by

$$C_{\mathrm{total}} = C_{\min} + kC_{\Delta}$$

where k is in the range of 0–15. In order to reduce the switch parasitic effect on the filter response, the tunable capacitor array in the feedback path has been arranged to have all the switches connect to the opamp virtual ground, as shown in Fig. 10. The opamp used in the filter stages is similar to the D/A two-stage opamp (Fig. 9) except that the output source-follower stage was omitted.

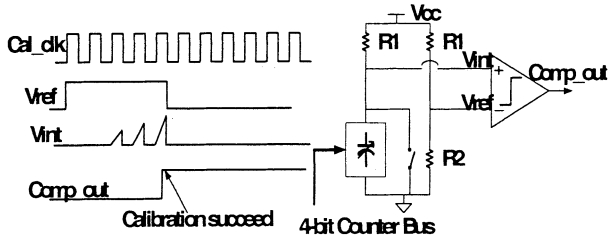


Fig. 11. Block and timing diagram of the calibration circuit.

The cutoff frequency of the active-RC filter is determined by the absolute values of R and C. However, the process variation of RC values could be as high as $+/-40\%$. Thus, an on-chip calibration circuit is needed to tune the cutoff frequency to the target specifications. The calibration circuit proposed (Fig. 11) uses a simple RC integrator to charge the capacitor to a certain voltage level (half clock cycle charge, half clock cycle discharge) and then compare the integrated value with a reference voltage. If the integrated voltage is larger than the reference voltage, then the comparator is triggered and the calibration has succeeded. The reference voltage $V_{\rm ref}$ is given by

$$V_{\rm ref} = V_{cc}(1 - e^{-T/2R_1C_{\rm total}}) - \Delta V_{\rm comp}$$

where T is the calibration clock period and $\Delta V_{\rm comp}$ is the offset error of the comparator. During the calibration process, the 4-bit tunable capacitor array is downcounted from its largest capacitor value to its smallest value. This corresponds to $V_{\rm int}$ starting from the lowest value, increasing code by code as the capacitor value decreases until $V_{\rm int}$ exceeds $V_{\rm ref}$. This triggers the comparator and terminates the calibration process.

C. TX PGA

The PGA is used to allow the AFE to interface to a wide range of RF chipsets [9]. The proposed PGA is implemented with five different gain levels. The PGA output common mode voltage $V\rm cm$ could be varied externally depending on the required $V\rm cm$ by the RF vendor. Since two PGAs are required for the I and Q signal paths, it is common to perform a calibration process on the signal's amplitude and phase to correct for any process-induced variation. But given that the transmitted signal bandwidth is relatively small (< 3 MHz) and with careful layout balancing for the I and Q blocks, no phase correction is necessary to meet the desired phase error spec. Thus, only amplitude offset error correction was performed for the TX signal path. The block diagram of the PGA with the power-on offset calibration circuit is shown in Fig. 12. After the TX path is powered on, a full path offset correction process is performed as follows. At the input of the TX D/A, a mid-code dc signal is applied and the PGA differential outputs are compared. The result of this comparison is sent to a control block where control bits are used to adjust the value of a programmable resistor string (PRS). This PRS serves as a means to create an artificial offset at the opamp inputs to counteract the original output differential offset. A binary search algorithm is used to ensure fast convergence of the offset calibration process.

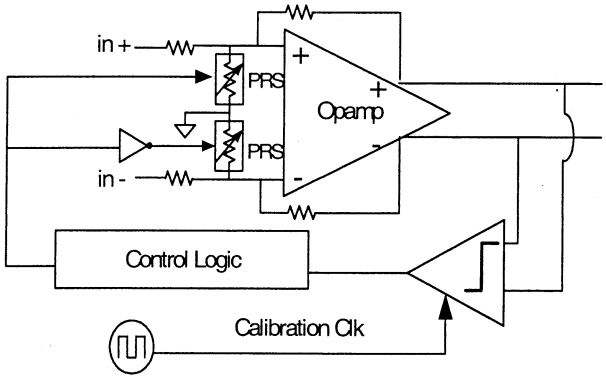


Fig. 12. PGA block diagram including the power-on offset calibration.

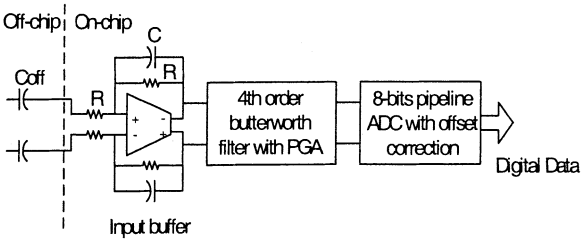


Fig. 13. Block diagram of the receiver.

IV. Receiver (RX) Design

A block diagram showing the different stages of the AFE receiver is shown in Fig. 13. The first stage of the RX is an input buffer that precedes a filter/PGA combination. An A/D with offset correction D/A then follows. The following discussion will focus on the input buffer design issues.

In general, dc offset is widely known to be a problem in direct downconversion receivers. This is because the value of dc offset could be several times higher than the desired signal, thereby causing early saturation of the high-gain stages. Since the WCDMA signal has low dc content, a high-pass filter at the front-end of the receiver can be used to cancel the dc offset. Typically, a combination of an off-chip capacitor $C_{\rm off}$ and a high input resistance inside the AFE receiver realize this high-pass filter. Since this high resistance cannot be implemented as part of the filter, an input buffer is used to provide this resistance, as shown in Fig. 13.

Although using a buffer at the input stage solves the dc offset problem, this architecture suffers from increased IMD because of the input buffer finite linearity. Intermodulation (IM) is a troublesome effect that arises when two signals with different frequencies are applied to a system that exhibits nonlinearity. The effect of third-order IM is shown in Fig. 14(a), where a weak signal accompanied by two strong high-frequency interferers passes through a nonlinear system, causing the third-order IM product to fall in the band of interest and distorting the desired signals. Once the IM product is generated from the buffer stage nonlinearity, it cannot be differentiated or removed from the desired signal using the following filter. The IMD level can be significantly reduced if the input stage is realized by a low-pass filter instead of the traditional unity gain buffer. A small capacitor C is included in the feedback path of the input buffer

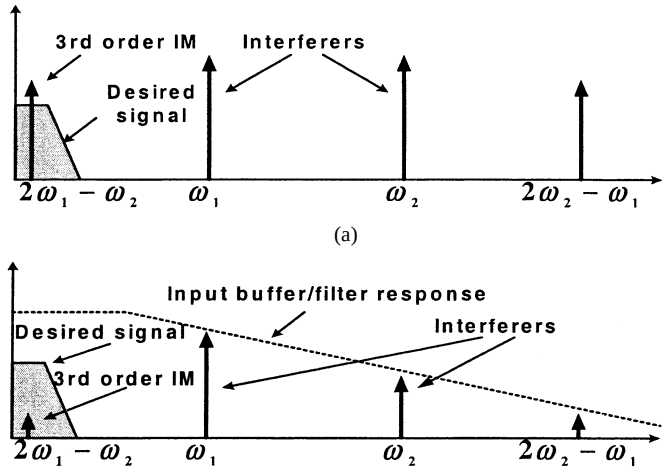


Fig. 14. Corruption of the desired signal due to third-order IM effect. (a) Using buffer without a filter at the input stage. (b) Using a buffer with added single pole filter at the input stage.

to form a single pole filter, as shown in Fig. 13. The low-pass cutoff frequency of this single-pole RC filter is placed outside the desired bandwidth while guaranteeing adequate attenuation of the high-frequency interferers, as shown in Fig. 14(b).

Given the traditional input buffer stage (no filtering), the IMD level at the A/D output was measured at -6 dBc. However, the IMD level dropped to -46 dBc after the addition of the single-pole filter to the buffer. This 40-dB drop represents a significant improvement in the IMD level of the whole receiver chain.

The remaining part of the receiver uses a fourth-order Butterworth filter with four programmable gain levels to provide for flexible RF front-end selection. Although this filter is mainly used for anti-aliasing, it also functions as a channel select filter. The RX filter architecture is similar to the one used in the TX. Following the filter is an 8-bit 15.36-MS/s pipelined A/D with built-in offset correction circuit. The offset correction is performed using a multibit D/A inside the A/D sample-and-hold circuit.

V. Test Results

The die photo for the integrated WCDMA AFE and audio Codec is shown in Fig. 15. The AFE occupies an area of 15 mm^2 and consumes 148 mW. In order to reduce the crosstalk between transmit and receive chains, the two paths and their associated external pins have been separated by the auxiliary A/D and D/A (Fig. 15). Furthermore, separate power-supply pins were used for the RX and TX paths. To increase the signal dynamic range over the chip background noise and achieve higher signal-to-noise ratio, all analog inputs/outputs are processed in a differential manner. Special care was taken in the package design to avoid any crosscoupling between the RX and TX signals. Both the AFE and audio Codec are operated through an on-chip digital interface, which is part of baseband modem.

The AFE on this chip was tested independent of the audio Codec. A summary of the AFE measured results is provided in Table I. To our knowledge, this is the first published results for a WCDMA AFE. A 300-kHz sine wave was applied to the input

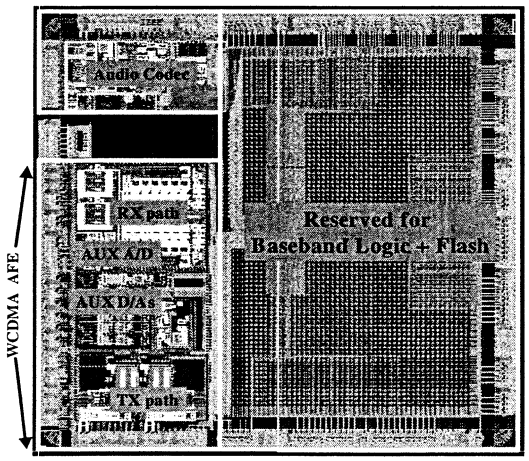


Fig. 15. Die photo for the WCDMA AFE and audio Codec.

TABLE I
AFE Performance Summary

TX Full Path (300KHz sine output)	
SFDR / SINAD	63.23dB / 55.40dB
SNR / ENOB	56.51dB / 9.1 bits
THD	-61.87dB
TX D/A:	
DNL	0.44 LSB
INL	0.60 LSB
TX Filter:	
Passband Flatness	< 0.2dB
THD	< -70dB
Cutoff Frequency Error	1.1 %
RX Full Path (1.2MHz sine input)	
SFDR / SINAD	64.36dB / 46.82dB
SNR / ENOB	46.86dB / 7.49 bits
AFE Summary	
Area	15 mm^2
Supply V / I	2.7V / 55mA

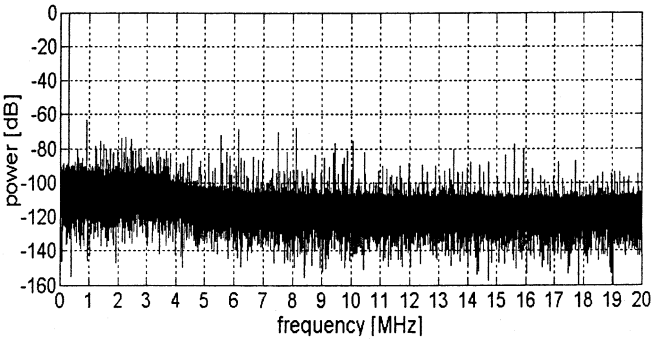


Fig. 16. TX channel output with a 300-kHz sine wave signal applied at the TX input.

of the TX channel and the measured output of the TX channel full path (D/A + Filter + PGA) is shown in Fig. 16. The peak spur signal is shown at 63.23 dB below the carrier. The THD of the channel full-scale output is measured at -61.87 dB. The full TX path achieves 9.1 effective number of bits at the carrier frequency of 300 kHz. Static linearity measurements for the TX D/A are shown in Fig. 17. The worst case DNL and INL are measured at 0.44 LSB and 0.60 LSB, respectively. This result

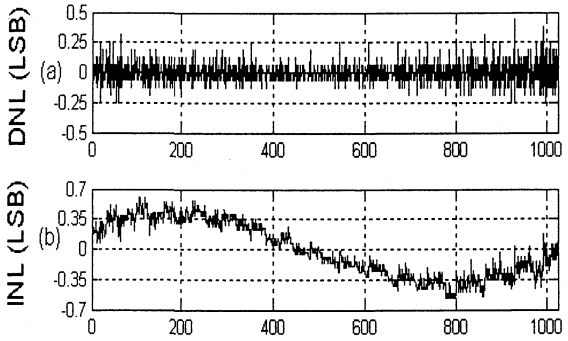


Fig. 17. Plot of the measured TX D/A. (a) DNL. (b) INL.

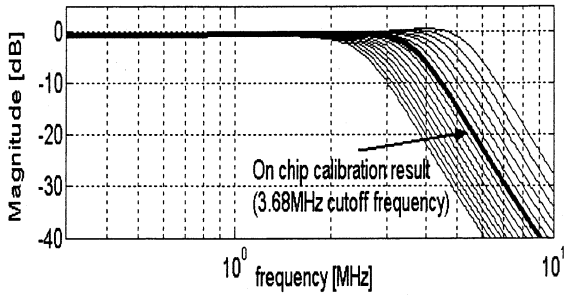


Fig. 18. Measured TX filter response across the entire turning range. Dark curve highlights the measured response after calibration.

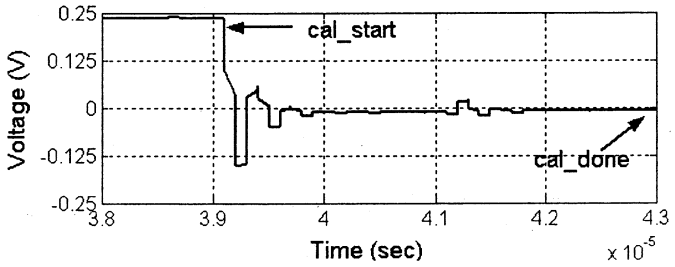


Fig. 19. Measured PGA offset during the calibration process.

translates to a near ideal 10-bit D/A performance without the use of trimming or calibration. Thus demonstrating the design robustness of the segmented R-2R topology and random-walk technique. On the dynamic side, the D/A settling time is measured at 51.2 ns.

The TX filter frequency response across the entire tuning range is shown in Fig. 18. The filter tuning bits were manually varied in single steps from all 0's to all 1's and the results were recorded. The measured cutoff frequency varied from 2.43 to 5.62 MHz, which is very close to the simulated range (2.50 to 6.07 MHz).The single calibrated result is highlighted in Fig. 18, where the cutoff frequency is shown at 3.68 MHz, which is only 1.1% away from the 3.72-MHz target. The passband flatness is measured below 0.2 dB.

A real-time calibration was done for the PGA to verify the operation of the autocalibration process. Fig. 19 shows a captured snapshot of the PGA output while the calibration process is converging to the final value. Note that at the start of the calibration process, the offset of the TX differential outputs measures 235 mV. After the process self-terminates, the corrected offset voltage is measured at −6 mV.

VI. Conclusion

The AFE chip described in this work was first-time functional. Given such a complex chip, this success was attributed to the use of comprehensive mixed-signal validation before the chip tapeout. After extensive testing, the performance of the majority of the blocks was shown to exceed the required specifications. The effect of crosstalk was not observed between the different parts of the chip due to careful layout planning and package pin assignment. All the calibration circuits are shown to converge to the design target after the chip is powered on.

Acknowledgment

The authors would like to thank all the members of the Chandler Analog Development Center for their contribution to the design, layout, development, and test of this AFE, and the CCD-I team for provision of system level specifications and their continuous support throughout the development. Special thanks go to the Technology Development team for the delivery of superior first-time silicon, and the analog CAD team in CCE for their great support on silicon models and CAD environment.

References

[1] C. Wong, "A 3-V GSM baseband transmitter," *IEEE J. Solid-State Circuits*, vol. 34, pp. 725–730, May 1999.

[2] A. Fraval and F. Dell'ova, "A 10-bit 70-MHz 3.3-V CMOS 0.5-μm D/A converter for video applications," *IEEE Trans. Consumer Electron.*, vol. 41, pp. 875–879, Aug. 1995.

[3] J. Fournier and P. Senn, "A 130-MHz 8-bit CMOS video DAC for HDTV applications," *IEEE J. Solid-State Circuits*, vol. 26, pp. 1073–1077, Dec. 1991.

[4] L. Wang, Y. Fukatsu, and K. Watanabe, "A CMOS R-2R ladder digital-to-analog converter and its characterization," in *Proc. IEEE Instrumentation and Measurement Technology Conf.*, May 2001, pp. 1026–1031.

[5] G. Van der Plas *et al.*, "A 14-bit intrinsic accuracy Q2 random walk CMOS DAC," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1708–1718, Dec. 1999.

[6] A. Durham, W. Redman-White, and J. Hughes, "High-linearity continuous-time filter in 5-V VLSI CMOS," *IEEE J. Solid-State Circuits*, vol. 27, pp. 1270–1276, Sept. 1992.

[7] E. Baguley *et al.*, *Reference Data for Radio Engineers.* New York: Sams, 1975.

[8] Hughes, "Analog techniques for very large scale integration," Ph.D. dissertation, Southampton Univ., Southampton, U.K., 1992.

[9] K. R. Lakshmikumar *et al.*, "Baseband codec for digital cellular telephony," *IEEE J. Solid-State Circuits*, vol. 26, pp. 1951–1958, Dec. 1991.

Waleed Khalil was born in Cairo, Egypt, in 1968. He received the B.S. and M.S. degrees in electrical engineering from the University of Minnesota, Minneapolis, in 1992 and 1993, respectively.

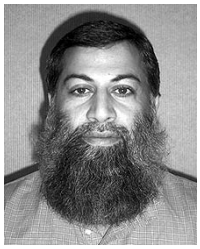
He joined Intel Corporation, Chandler, AZ, in 1993, where he worked on CMOS sensors, high-speed memory, and data converters. He was the Technical Leader for the WCDMA AFE project. He is currently working on frequency synthesizers for RF applications.

Tsung-Yuan Chang received the B.Sc. degree from Tatung Institute of Technology, Taipei, Taiwan, R.O.C., the M.S. degree from Syracuse University, Syracuse, NY, and the Ph.D. degree from The Ohio State University, Columbus, in 1988, 1992, and 1998, respectively, all in electrical engineering.

In 1999, he joined Lucent Technology, Columbus, OH, where he was involved in the testing of cellular base stations. In 2000, he joined Intel Corporation, Chandler, AZ, to develop CMOS-based analog transceiver circuits for cellular handsets. He has two patents pending.

Xuewen Jiang received the B.S. and M.S. degrees in materials science from Shanghai Jiao Tong University, Shanghai, China, in 1994 and 1997, respectively, and the M.S. and Ph.D. degrees in electrical engineering from the University of Minnesota, Minneapolis-St. Paul, in 1999 and 2001, respectively.

He has been with Intel Corporation, Chandler, AZ, since 2000. His research interests include MEMS devices fabrication techniques, digital readout electronics for solid-state sensing devices, high-speed data conversion circuitry, and VLSI current-mode testing.



Syed R. Naqvi was born in Karachi, Pakistan, in 1965. He received the B.S degree in electrical engineering from NED University of Engineering and Technology, Karachi, in 1989 and the M.S. degree in electrical engineering from the Arizona State University, Tempe, in 1993, where he is currently working toward the Ph.D. degree in RF circuits.

He is currently a Staff RF/Analog Engineer for the Wireless Communication and Computing group, Intel Corporation, Chandler, AZ. His research interests include digital module design, clocking, frequency dividers, bandgaps, and D/A and modulator design.

Babak Nikjou was born in Tehran, Iran, in 1963. He received the B.S. and M.S. degrees in electrical engineering from Arizona State University, Tempe, in 1986 and 1989, respectively, where he is currently working toward the Ph.D. degree in the area of RF circuits.

He is currently the Analog Design Manager for the Wireless Communication and Computing group, Intel Corporation, Chandler, AZ. His research interests include CMOS sensors, high-speed cache memory design, and mixed-signal validation.

James Tseng was born in Changhua, Taiwan, R.O.C., in 1976. He received the B.S. and M.S.E. degrees in electrical engineering from Arizona State University, Tempe, in 1998 and 1999, respectively.

Since 2000, he has been with Intel Corporation, Chandler, AZ, working on developing data converters and other mixed-signal blocks for use in cell phones.

射 频 和 天 线 设 计 培 训 课 程 推 荐

易迪拓培训(www.edatop.com)由数名来自于研发第一线的资深工程师发起成立，致力并专注于微波、射频、天线设计研发人才的培养；我们于 2006 年整合合并微波 EDA 网(www.mweda.com)，现已发展成为国内最大的微波射频和天线设计人才培养基地，成功推出多套微波射频以及天线设计经典培训课程和 ADS、HFSS 等专业软件使用培训课程，广受客户好评；并先后与人民邮电出版社、电子工业出版社合作出版了多本专业图书，帮助数万名工程师提升了专业技术能力。客户遍布中兴通讯、研通高频、埃威航电、国人通信等多家国内知名公司，以及台湾工业技术研究院、永业科技、全一电子等多家台湾地区企业。

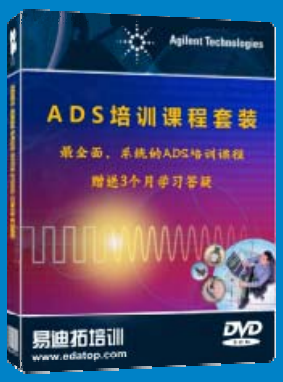
易迪拓培训课程列表：http://www.edatop.com/peixun/rfe/129.html

射频工程师养成培训课程套装

该套装精选了射频专业基础培训课程、射频仿真设计培训课程和射频电路测量培训课程三个类别共 30 门视频培训课程和 3 本图书教材；旨在引领学员全面学习一个射频工程师需要熟悉、理解和掌握的专业知识和研发设计能力。通过套装的学习，能够让学员完全达到和胜任一个合格的射频工程师的要求…

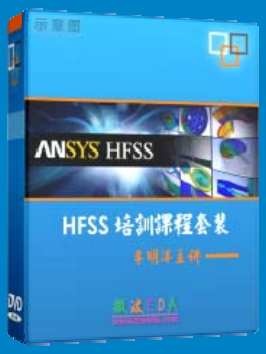
课程网址：http://www.edatop.com/peixun/rfe/110.html

ADS 学习培训课程套装



该套装是迄今国内最全面、最权威的 ADS 培训教程，共包含 10 门 ADS 学习培训课程。课程是由具有多年 ADS 使用经验的微波射频与通信系统设计领域资深专家讲解，并多结合设计实例，由浅入深、详细而又全面地讲解了 ADS 在微波射频电路设计、通信系统设计和电磁仿真设计方面的内容。能让您在最短的时间内学会使用 ADS，迅速提升个人技术能力，把 ADS 真正应用到实际研发工作中去，成为 ADS 设计专家...

课程网址： http://www.edatop.com/peixun/ads/13.html



HFSS 学习培训课程套装

该套课程套装包含了本站全部 HFSS 培训课程，是迄今国内最全面、最专业的 HFSS 培训教程套装，可以帮助您从零开始，全面深入学习 HFSS 的各项功能和在多个方面的工程应用。购买套装，更可超值赠送 3 个月免费学习答疑，随时解答您学习过程中遇到的棘手问题，让您的 HFSS 学习更加轻松顺畅…

课程网址：http://www.edatop.com/peixun/hfss/11.html

CST 学习培训课程套装

该培训套装由易迪拓培训联合微波 EDA 网共同推出，是最全面、系统、专业的 CST 微波工作室培训课程套装，所有课程都由经验丰富的专家授课，视频教学，可以帮助您从零开始，全面系统地学习 CST 微波工作的各项功能及其在微波射频、天线设计等领域的设计应用。且购买该套装，还可超值赠送 3 个月免费学习答疑…

课程网址：http://www.edatop.com/peixun/cst/24.html

HFSS 天线设计培训课程套装

套装包含 6 门视频课程和 1 本图书，课程从基础讲起，内容由浅入深，理论介绍和实际操作讲解相结合，全面系统的讲解了 HFSS 天线设计的全过程。是国内最全面、最专业的 HFSS 天线设计课程，可以帮助您快速学习掌握如何使用 HFSS 设计天线，让天线设计不再难…

课程网址：http://www.edatop.com/peixun/hfss/122.html

13.56MHz NFC/RFID 线圈天线设计培训课程套装

套装包含 4 门视频培训课程，培训将 13.56MHz 线圈天线设计原理和仿真设计实践相结合，全面系统地讲解了 13.56MHz 线圈天线的工作原理、设计方法、设计考量以及使用 HFSS 和 CST 仿真分析线圈天线的具体操作，同时还介绍了 13.56MHz 线圈天线匹配电路的设计和调试。通过该套课程的学习，可以帮助您快速学习掌握 13.56MHz 线圈天线及其匹配电路的原理、设计和调试…

详情浏览：http://www.edatop.com/peixun/antenna/116.html

我们的课程优势：

※ 成立于 2004 年，10 多年丰富的行业经验，

※ 一直致力并专注于微波射频和天线设计工程师的培养，更了解该行业对人才的要求

※ 经验丰富的一线资深工程师讲授，结合实际工程案例，直观、实用、易学

联系我们：

※ 易迪拓培训官网：http://www.edatop.com

※ 微波 EDA 网：http://www.mweda.com

※ 官方淘宝店：http://shop36920890.taobao.com