Application Note AN4137

Design Guidelines for Off-line Flyback Converters Using FPS

Abstract

This paper presents practical design guidelines for off-line flyback converter employing FPS (Fairchild Power Switch). Switched mode power supply (SMPS) design is inherently time consuming job requiring many trade-offs and iteration with a large number of design variables.
The step-by-step design procedure described in this paper helps the engineers to design SMPS easily. In order to make the design process more efficient, a software design tool, **FPS design assistant** that contains all the equations described in this paper is also provided.

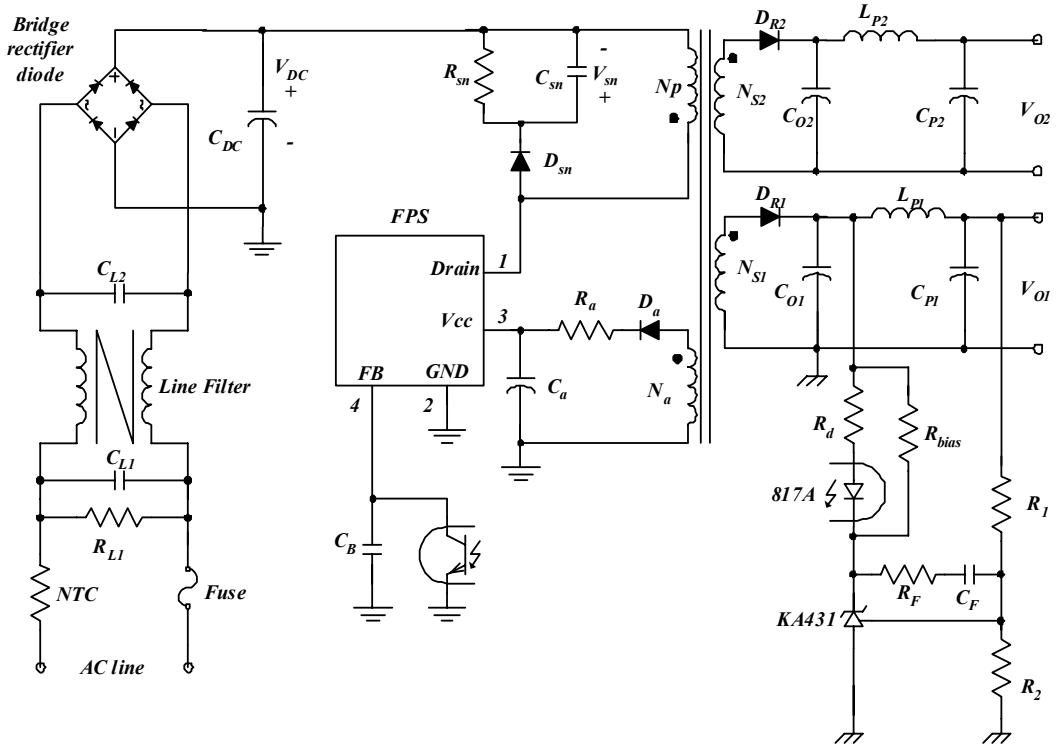


Figure 1. Basic Off-line Flyback Converter Using FPS

1. Introduction

Figure 1 shows the schematic of the basic off-line flyback converter using FPS, which also serves as the reference circuit for the design process described in this paper. Because the MOSFET and PWM controller together with various additional circuits are integrated into a single package, the design of SMPS is much easier than the discrete MOSFET and PWM controller solution. This paper provides step-by-step design procedure for FPS based off-line flyback converter, which includes transformer design, output filter design, component selection and closing the feedback loop. The design procedure described herein is general enough to be applied to various applications. The design procedure presented in this paper is also implemented in a software design tool (FPS design assistant) to enable the engineer to finish SMPS design in a short time. In the appendix, a step-by-step design example using the software tool is provided.

2. Step-by-step Design Procedure

In this section, design procedure is presented using the schematic of the figure 1 as the reference. In general, most FPS has the same pin configuration from pin 1 to pin 4, as shown in figure 1.

(1) STEP-1 : Determine the system specifications

- Line voltage range (V_{line}^{min} and V_{line}^{max}).

- Line frequency (f_L).

- Maximum output power (P_o).

- Estimated efficiency (E_{ff}) : It is required to estimate the power conversion efficiency to calculate the maximum input power. If no reference data is available, set E_{ff} = 0.7~0.75 for low voltage output applications and E_{ff} = 0.8~0.85 for high voltage output applications.

With the estimated efficiency, the maximum input power is given by

$$P_{in} = \frac{P_o}{E_{ff}} \quad (1)$$

For multiple output SMPS, the load occupying factor for each output is defined as

$$K_{L(n)} = \frac{P_{o(n)}}{P_o} \quad (2)$$

where $P_{o(n)}$ is the maximum output power for n-th output. For single output SMPS, $K_{L(1)}$=1.

Considering the maximum input power, choose the proper FPS. The FPS lineup with proper power rating is also included in the software design tool.

(2) STEP-2 : Determine DC link capacitor (C_{DC}) and the DC link voltage range.

The maximum DC link voltage ripple is obtained as

$$\Delta V_{DC}^{max} = \frac{P_{in} \cdot (1 - D_{ch})}{\sqrt{2}V_{line}^{min} \cdot 2f_L \cdot C_{DC}} \quad (3)$$

where D_{ch} is the DC link capacitor charging duty ratio defined as shown in figure 2, which is typically about 0.2. For universal input range (85-265Vrms), it is proper to set ΔV_{DC}^{max} as 10~15% of $\sqrt{2}V_{line}^{min}$.

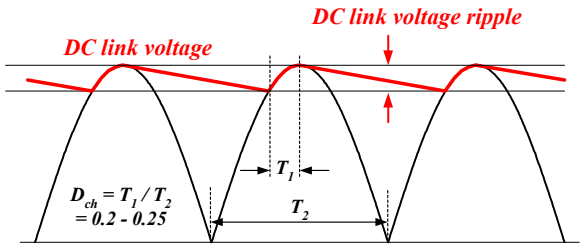


Figure 2. DC Link Voltage Waveform

With the resulting maximum voltage ripple, the minimum and maximum DC link voltages are given as

$$V_{DC}^{min} = \sqrt{2}V_{line}^{min} - \Delta V_{DC}^{max} \quad (4)$$

$$V_{DC}^{max} = \sqrt{2}V_{line}^{max} \quad (5)$$

(3) STEP-3 : Determine the maximum duty ratio (D_{max}).

For CCM operation, it is recommended to set D_{max} to be smaller than 0.5 in order to avoid sub-harmonic oscillation. Then, the output voltage reflected to the primary (V_{RO}) and the maximum nominal MOSFET voltage (V_{ds}^{nom}) are obtained as.

$$V_{RO} = \frac{D_{max}}{1 - D_{max}} \cdot V_{DC}^{min} \quad (6)$$

$$V_{ds}^{nom} = \sqrt{2}V_{line}^{max} + V_{RO} \quad (7)$$

As can be seen in equation (6) and (7), the voltage stress on MOSFET can be reduced, by decreasing D_{max}. However, this increases the voltage stresses on the rectifier diodes in the secondary side. Therefore, it is desirable to set D_{max} as large as possible if there is enough margin in the MOSFET voltage rating. The typical value for D_{max} is 0.45.

(4) STEP-4 : Determine the transformer primary side inductance (L_m).

Flyback converter has two kinds of operation mode ; continuous conduction mode (CCM) and discontinuous conduction mode (DCM). The operation mode changes as the load condition and input voltage vary. Therefore, the inductance of the transformer primary side is determined in full load and minimum input voltage condition as

$$L_m = \frac{(V_{DC}^{min} \cdot D_{max})^2}{2P_{in}f_s K_{RF}} \quad (8)$$

where f_s is the switching frequency and K_{RF} is the ripple factor defined as shown in figure 3. For DCM operation, K_{RF} = 1 and for CCM operation K_{RF} < 1. For universal input range, it is reasonable to set K_{RF} = 0.3-0.5.

The maximum peak current and RMS current of MOSFET are obtained as

$$I_{ds}^{peak} = I_{EDC} + \frac{\Delta I}{2} \quad (9)$$

$$I_{ds}^{rms} = \sqrt{\left[3(I_{EDC})^2 + \left(\frac{\Delta I}{2}\right)^2\right]\frac{D_{max}}{3}} \quad (10)$$

$$\text{where} \quad I_{EDC} = \frac{P_{in}}{V_{DC}^{min} \cdot D_{max}} \qquad (11)$$

$$\text{and} \quad \Delta I = \frac{V_{DC}^{min} D_{max}}{L_m f_s} \qquad (12)$$

Check if MOSFET maximum peak current (I_{ds}^{peak}) is below the pulse-by-pulse current limit level of the FPS (I_{lim}).

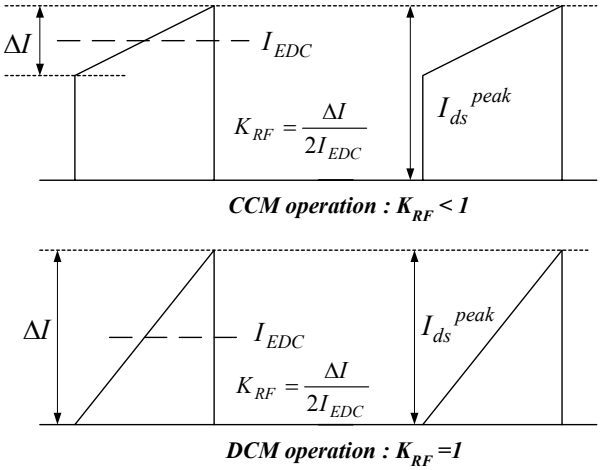


Figure 3. MOSFET Drain Current and Ripple Factor(K_{RF})

(5) STEP-5 : Determine the proper core and the minimum primary turns.

Actually, the initial selection of the core is bound to be crude since there are too many variables. One way to select the proper core is refer to the manufacture's core selection guide. If there is no proper reference, use the following equation as a starting point.

$$A_p = A_w A_e = \left[\frac{L_m \times I_{ds}^{peak} I_{ds}^{rms} \times 10^4}{450 \times 0.2 \times \Delta B}\right]^{1.143} \times 10^4 (mm^4) \qquad (13)$$

where A_w is the window area and A_e is the cross sectional area of the core in mm^2 as shown in figure 4. ΔB is the maximum flux density swing in tesla in normal operation, which is typically 0.3-0.35 T for most power ferrite cores.

With a chosen core, the minimum number of turns for the transformer primary side to avoid saturation is given by

$$N_P^{min} = \frac{L_m I_{lim}}{B_{sat} A_e} \times 10^6 \quad (turns) \qquad (14)$$

where I_{lim} is the FPS current limit level, B_{sat} is the saturation flux density in tesla. If there is no reference data, use B_{sat} =0.35-0.4 T.

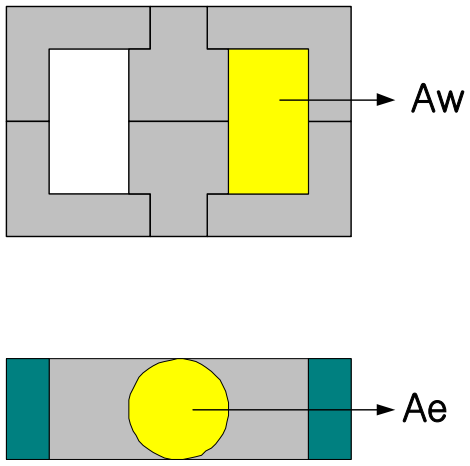


Figure 4. Window Area and Cross Sectional Area

(6) STEP-6 : Determine the number of turns for each output.

First, determine the turns ratio between the primary side and the feedback controlled secondary side as a reference.

$$n = \frac{N_P}{N_{s1}} = \frac{V_{R0}}{V_{o1} + V_{F1}} \qquad (15)$$

where N_p and N_{s1} are the number of turns for primary side and reference output, respectively. V_{o1} is the output voltage and V_{F1} is the diode forward voltage drop of the reference output.

Then, determine the proper integer numbers for N_{s1} so that resulting Np is larger than N_p^{min} obtained from equation (14). Sometimes the resulting N_p may be too larger than N_p^{min}, which forces to change the core size for a big one. If it is not possible to change the core due to cost or size constraint, go back to step 4 and reduce L_m by increasing the ripple factor (K_{RF}). Then, the resulting minimum number of turns of the primary side will be decreased.

The numer of turns for the the other output (n-th output) is determined as

$$N_{s(n)} = \frac{V_{o(n)} + V_{F(n)}}{V_{o1} + V_{F1}} \cdot N_{s1} \quad (turns) \qquad (16)$$

The numer of turns for Vcc winding is determined as

$$N_a = \frac{V_{cc}^* + V_{Fa}}{V_{o1} + V_{F1}} \cdot N_{s1} \quad (turns) \qquad (17)$$

where V_{cc}* is the nominal voltage for V_{cc} and V_{Fa} is the diode forward voltage drop. Since V_{cc} increases as the output load increases, it is proper to set V_{cc}* as V_{cc} start voltage to avoid the over voltage protection during the normal operation.

With the determined turns of the primary side, the gap length of the core is obtained as

$$G = 40\pi A_e\left(\frac{N_P^2}{1000L_m} - \frac{1}{A_L}\right) \quad (mm) \qquad (18)$$

where A_L is the AL-value with no gap in nH/turns^2.

(7) STEP-7 : Determine the wire diameter for each winding based on the rms current of the each output.

The rms current of the n-th scondary winding is obtained as

$$I_{sec(n)}^{rms} = I_{ds}^{rms}\sqrt{\frac{1-D_{max}}{D_{max}}}\cdot\frac{V_{RO}\cdot K_{L(n)}}{(V_{o(n)}+V_{F(n)})} \qquad (19)$$

where $K_{L(n)}$ is the load occupying factor for n-th output defined in equation (2).

The current density is typically 5A/mm^2 when the wire is long (>1m). When the wire is short with small number of turns, current density of 6-10 A/mm^2 is also acceptable. Avoid using wire with diameter larger than 1 mm to avoid severe eddy current losses and to make winding easier.

For high current output, it is better to use parallel winding with multiple strands of thinner wire to minimize skin effect.

Check if the winding window area of the core is enough to accommodate the wires. The required window area is given by

$$A_w = A_c / A_F \qquad (20)$$

where A_c is the actual conductor area and K_F is the fill factor. Typically the fill factor is 0.2-0.3.

(8) STEP-8 : Choose the rectifier diode in the secondary side based on the voltage and current ratings.

The maximum voltage and the rms current of the rectifier diode of the n-th output are obtained as

$$V_{D(n)} = V_{o(n)} + \frac{V_{DC}^{max}\cdot(V_{o(n)}+V_{F(n)})}{V_{RO}} \qquad (21)$$

$$I_{D(n)}^{rms} = I_{ds}^{rms}\sqrt{\frac{1-D_{max}}{D_{max}}}\cdot\frac{V_{RO}K_{L(n)}}{(V_{o(n)}+V_{F(n)})} \qquad (22)$$

(9) STEP-9 : Determine the output capacitor considering the voltage and current ripple.

The ripple current of the n-th output capacitor is obtained as

$$I_{cap(n)}^{rms} = \sqrt{(I_{D(n)}^{rms})^2 - I_{o(n)}^2} \qquad (23)$$

where *Io(n)* is the load current of n-th output. The ripple current should be equal to or smaller than the ripple current specification of the capacitor.

The voltage ripple on n-th output is given by

$$\Delta V_{o(n)} = \frac{I_{o(n)}D_{max}}{C_{o(n)}f_s} + \frac{I_{ds}^{peak}V_{RO}R_{C(n)}K_{L(n)}}{(V_{o(n)}+V_{F(n)})} \qquad (24)$$

where $C_{o(n)}$ is the capacitance and $R_{c(n)}$ is the effective series resistance (ESR) of the n-th output capacitor.

Sometimes it is impossible to meet the ripple specification with a single output capacitor due to the high ESR of the electrolytic capacitor. Then, additional LC filter (post filter) can be used. When using the post filter, be careful not to place the corner frequency too low. Too low corner frequency may make the system unstable or limit the control bandwidth. It is proper to set the corner frequency of the post filter to be around 1/10~1/5 of the switching frequency.

(10) STEP-10 : Design the RCD snubber.

The power loss of the snubber network in normal operation is obtained as

$$Loss_{sn} = \frac{V_{sn}^2}{R_{sn}} = \frac{1}{2}L_{lK}(I_{ds}^{peak})^2 f_s \qquad (25)$$

where L_{lk} is the primary side leakage inductance, V_{sn} is the snubber capacitor voltage in normal operation and R_{sn} is the snubber resistor. Based on the power loss, the snubber resistor with proper rated wattage should be chosen. The snubber capacitor voltage should be larger than the reflected output voltage (V_{RO}). It is typical to set V_{sn} to be 50~100V higher than V_{RO}. The ripple of the snubber capacitor voltage in normal operation is obtained as

$$\Delta V_{sn} = \frac{V_{sn}}{C_{sn}R_{sn}f_s} \qquad (26)$$

In general, 5-10% ripple is reasonable.

The maximum snubber capacitor voltage during transient or over load situation is obtained as

$$V_{sn}^{max} = \sqrt{\frac{1}{2}R_{sn}L_{lk}f_s}\cdot I_{lim} \qquad (27)$$

Then, the maximum voltage stress of MOSFET is given by

$$V_{ds}^{max} = \sqrt{2}V_{line}^{max} + V_{sn}^{max} \qquad (28)$$

Design V_{ds}^{max} to be below 90 % of the rated voltage of MOSFET. Be careful when measuring the primary side leakage inductance. By simply measuring the primary side inductance with other outputs shorted, somewhat larger value of leakage inductance is obtained since the secondary side leakage inductance for each output is reflected to the primary side.

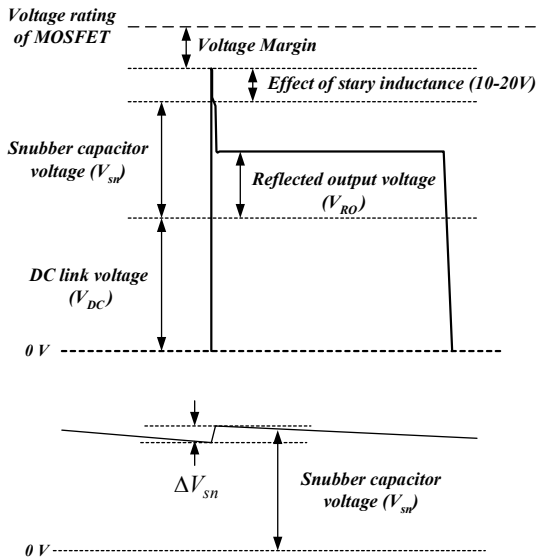


Figure 5. MOSFET voltage and snubber capacitor voltage

(11) STEP-11 : Design the feed back loop.

Since FPS employs current mode control as shown in figure 6, the feedback loop can be simply implemented with a one-pole and one-zero compensation circuit.

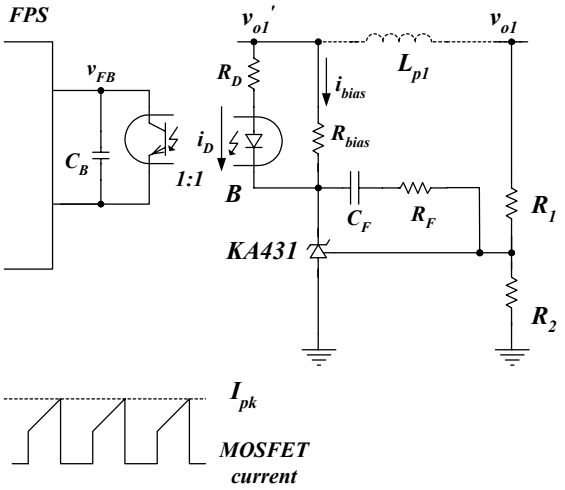


Figure 6. Control Block Diagram

For CCM operation, the control-to-output transfer function of the flyback converter using FPS is given by

$$G_{vc} = \frac{\hat{v}_{o1}}{\hat{v}_{FB}} = \frac{K \cdot R_L V_{DC}(N_p/N_{s1})}{2V_{RO} + v_{DC}} \cdot \frac{(1 + s/w_z)(1 - s/w_{rz})}{1 + s/w_p} \quad (29)$$

where V_{DC} is the DC input voltage, R_L is the effective total load resistance of the controlled output defined as V_{o1}^2/P_o,

$$w_z = \frac{1}{R_{c1}C_{o1}},\ w_{rz} = \frac{R_L(1-D)^2}{DL_m(N_{s1}/N_p)^2} \text{ and } w_p = \frac{(1+D)}{R_L C_{o1}}$$

When the converter has more than one output, the DC and low frequency control-to-output transfer function are proportional to the parallel combination of all load resistance, adjusted by the square of the turns ratio. Therefore, the effective load resistance is used in equation (29) instead of the actual load resistance of V_{o1}.

The voltage-to-current conversion ratio of FPS, K is defined as

$$K = \frac{I_{pk}}{V_{FB}} = \frac{I_{lim}}{3} \quad (30)$$

where I_{pk} is the peak drain current and V_{FB} is the feedback voltage for a given operating condition.

Notice that there is right half plane (RHP) zero (w_{rz}) in the control-to-output transfer function of equation (29). Because the RHP zero reduces the phase by 90 degrees, the crossover frequency should be placed below the RHP zero.

Figure 7 shows variation of CCM flyback converter control-to-output transfer function according to the input voltage. As can be seen, the system poles and zeros together with the DC gain change according to input voltage. The gain is highest in high input voltage condition and the RHP zero is lowest in low input voltage condition.

Figure 8 shows variation of CCM flyback converter control-to-output transfer function according to the load. As can be seen, the low frequency gain does not change according to the load condition and the RHP zero is lowest in full load condition.

For DCM operation, the control-to-output transfer function of the flyback converter using FPS is given by

$$G_{vc} = \frac{\hat{v}_{o1}}{\hat{v}_{FB}} = \frac{V_{o1}}{V_{FB}} \cdot \frac{(1 + s/w_z)}{(1 + s/w_p)} \quad (31)$$

$$\text{where} \quad w_z = \frac{1}{R_{c1}C_{o1}},\ w_p = 2/R_L C_{o1}$$

Figure 9 shows the variation of the control-to-output transfer function of flyback converter in DCM according to the load. Contrary to the flyback converter in CCM, there is no RHP zero and the DC gain does not change as the input voltage varies. As can be seen, the overall gain except for the DC gain is highest in full load condition

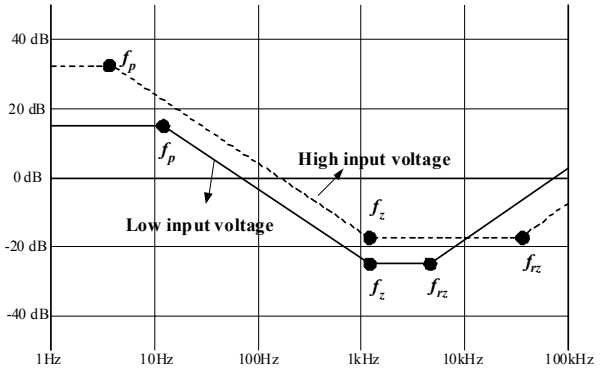


Figure 7. CCM flyback converter control-to output transfer function variation according to the input voltage

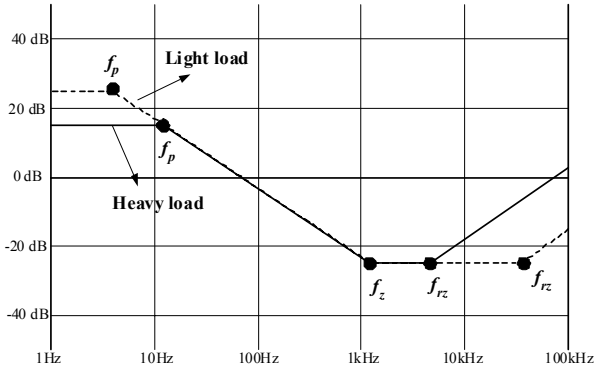


Figure 8. CCM flyback converter control-to output transfer function variation according to the load

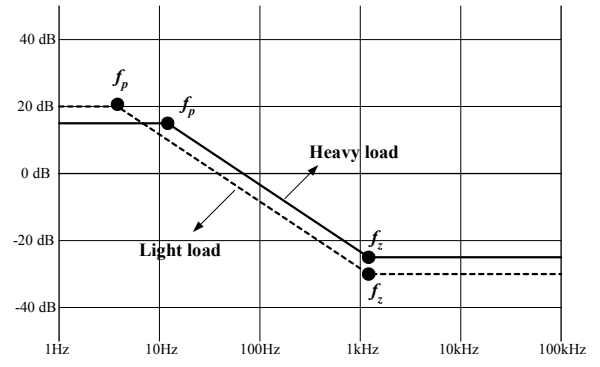


Figure 9. DCM flyback converter control-to output transfer function variation according to the load

The feedback compensation network transfer function of figure 6 is obtained as

$$\frac{\hat{v}_{FB}}{\hat{v}_{o1}} = -\frac{w_i}{s} \cdot \frac{1 + s/w_{zc}}{1 + 1/w_{pc}} \qquad (32)$$

$$\text{where } w_i = \frac{R_B}{R_1 R_D C_F s},\ w_{zc} = \frac{1}{(R_F + R_1)C_F},\ w_{pc} = \frac{1}{R_B C_B}$$

When the input voltage and the load current vary over wide range, it is not easy to determine the worst case for the feedback loop design. The gain together with zeros and poles move according to the operating condition. Moreover, converter operating in CCM enters into DCM as the load current decreases and/or input voltage increases.

One simple and practical way to this problem is designing the feedback loop for low input voltage and full load condition with enough phase and gain margin. For universal input range, the RHP zero is lowest in low input voltage and full load condition when the converter operates in CCM. While, the gain increases only about 6dB as the operating condition is changed from low line to high line condition. Therefore, by designing the feedback loop with more than 45 degrees phase margin in low line and full load condition, the stability all over the operation ranges can be guaranteed.

The procedure to design the feedback loop is as follows

(a) Determine the crossover frequency (f_c). For CCM mode flyback, set f_c below 1/3 of right half plane (RHP) zero to minimize the effect of RHP zero. For DCM mode f_c can be placed at higher frequency, since there is no RHP zero.

(b) When additional LC filter is employed, the crossover frequency should be placed below 1/3 of the corner frequency of the LC filter, since it introduces -180 degrees phase drop. Never place the crossover frequency beyond the corner frequency of the LC filter. If the crossover frequency is too close the corner frequency, the controller should be designed to have enough phase margin more than about 90 degress when ignoring the effect of post filter.

(c) Determine the DC gain of the compensator (w_i/w_{zc}) to cancel the control-to-output gain at f_c.

(d) Place compensator zero (f_{zc}) around $f_c/3$.

(e) Place compensator pole (f_{pc}) above $3f_c$.

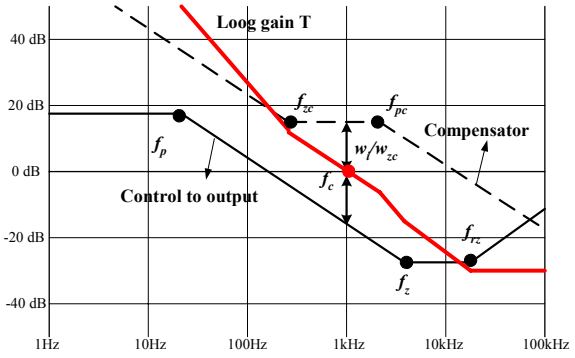


Figure 10. Compensator design

When determining the feedback circuit component, there are some restrictions as follows.

(a) The capacitor connected to feedback pin (CB) is related with the shutdown delay time in overload situation as

$$T_{delay} = (V_{SD} - 3) \cdot C_B / I_{delay} \quad (33)$$

where V_{SD} is the shutdown feedback voltage and I_{delay} is the shutdown delay current. These vales are given in the data sheet. In general, 10 ~ 100 ms delay time is proper for most applications. In some cases, the bandwidth may be limited due to the required delay time of the over load protection.

(b) The resistor R_{bias} and R_D used together with opto-coupler and KA431 should be designed to provide proper operating current for KA431 and to guarantee the full swing of the feedback voltage of FPS. In general, the minimum cathode voltage and current for KA431 are 2.5V and 1mA, respectively. Therefore, R_{bias} and R_D should be designed to satisfy the following conditions.

$$\frac{V_{o1} - V_{OP} - 2.5}{R_D} > I_{FB} \quad (34)$$

$$\frac{V_{OP}}{R_{bias}} > 1mA \quad (35)$$

where V_{OP} is opto-diode forward voltage drop, which is typically 1V and I_{FB} is the feedback current of FPS, which is typically 1mA. For example, R_{bias}< 1kΩ and R_D < 1.5kΩ for V_{o1}=5V.

- Summary of symbols -

A_w	: Window area of the core in mm^2
Ae	: Cross sectional area of the core in mm^2
B_{sat}	: Saturation flux density in tesla.
ΔB	: Maximum flux density swing in tesla in normal operation
C_o	: Capacitance of the output capacitor.
D_{max}	: Maximum duty cycle ratio
E_{ff}	: Estimated efficiency
f_L	: Line frequency
f_s	: Switching frequency
I_{ds}^{peak}	: Maximum peak current of MOSFET
I_{ds}^{rms}	: RMS current of MOSFET
I_{lim}	: FPS current limit level.
$I_{sec(n)}^{rms}$	: RMS current of the secondary winding for n-th output
$I_{D(n)}^{rms}$	: Maximum rms current of the rectifier diode for n-th output
$I_{cap(n)}^{rms}$	: RMS Ripple current of the output capacitor for n-th output
I_o	: Output load current
$K_{L(n)}$	: Load occupying factor for n-th output
K_{RF}	: Current ripple factor
L_m	: Transformer primary side inductance
$Loss_{sn}$	: Power loss of the snubber network in normal operation
L_{lk}	: Primary side leakage inductance of the transformer
N_p^{min}	: The minimum number of turns for the transformer primary side to avoid saturation
N_p	: Number of turns for primary side
N_{s1}	: Number of turns for the reference output
P_o	: Maximum output power
P_{in}	: Maximum input power
R_c	: Effective series resistance (ESR) of the output capacitor.
R_{sn}	: Snubber resistor
R_L	: Effective total output load resistor
V_{line}^{min}	: Minimum line voltage
V_{line}^{max}	: Maximum line voltage
V_{DC}^{min}	: Minimum DC link voltage
V_{DC}^{max}	: Maximum DC line voltage
V_{ds}^{nom}	: Maximum nominal MOSFET voltage
V_{o1}	: Output voltage of the reference output.
V_{F1}	: Diode forward voltage drop of the reference output.
V_{cc}^{*}	: Nominal voltage for Vcc
V_{Fa}	: Diode forward voltage drop of Vcc winding
ΔV_{DC}^{max}	: Maximum DC link voltage ripple
$V_{D(n)}$	: Maximum voltage of the rectifier diode for n-th output
$\Delta V_{o(n)}$	: Output voltage ripple for n-th output
V_{RO}	: Output voltage reflected to the primary
V_{sn}	: Snubber capacitor voltage in normal operation
ΔV_{sn}	: Snubber capacitor voltage ripple
V_{sn}^{max}	: Maximum snubber capacitor voltage during transient or over load situation
V_{ds}^{max}	: Maximum voltage stress of MOSFET

Appendix. Design Example Using FPS Design Assistant (1)

Target system : LCD monitor adaptor
- The height of SMPS is restricted (<20mm). The size of the heat sink is also limited.
- Input : universal input (85V-265Vrms)
- Output : 5V/2A, 12V/3A

FAIRCHILD SEMICONDUCTOR™

FPS Design Assistant ver.1.0 By Choi

Blue cell is the input parameters
Red cell is the output parameters

1. Define specifications of the SMPS

Minimum Line voltage (V_line.min)	85	V.rms
Maximum Line voltage (V_line.max)	265	V.rms
Line frequency (fL)	60	Hz

	Vo		Io		Po		KL	
1st output for feedback	5	V	2.4	A	12	W	25	%
2nd output	12	V	3	A	36	W	75	%
3rd output	0	V	0	A	0	W	0	%
4th output	0	V	0	A	0	W	0	%
5th output	0	V	0	A	0	W	0	%
6th output	0	V	0	A	0	W	0	%
Maximum output power (Po) =	48.0	W						
Estimated efficiency (Eff)	80	%						
Maximum input power (Pin) =	60.0	W						

2. Calculate the minimum input voltage

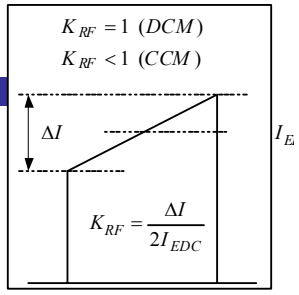
DC link capacitor	100	uF
DC link voltage ripple =	33	V
Minimum DC link voltage =	87	V
Maximum DC link voltage =	375	V

3. Determine Maximum duty ratio (Dmax)

Maximum duty ratio	0.45	
Maximum nominal MOSFET voltage =	446	V
Output voltage reflected to primary =	71	V

4. Determine transformer primary inductance (Lm)

Switching frequency of FPS (kHz)	67	kHz
Ripple factor	0.28	
Primary side inductance (Lm) =	680	uH
Maximum peak drain current =	1.96	A
RMS drain current	1.04	A
Maximum DC link voltage in CCM	197	V



5. Determine proper core and minimum primary turns

Current limit of FPS	2.20	A
Maximum flux density swing	0.35	T
Saturation flux density (Bsat)	0.42	T
Estimated AP value of core =	3929	mm^4
Cross sectional area of core (Ae)	58	mm^2
Minimum primary turns =	61.4	T

For a first step, EFD2525 is chosen
(Ae=58mm^2, Aw=77mm^2, Ap=4466mm^4)

6. Determine the numner of turns for each outputs

	Vo		VF			# of turns	
Vcc (Use Vcc start voltage)	12	V	1.2	V	12	=>	12 T
1st output for feedback	5	V	0.5	V	5	=>	5 T
2nd output	12	V	1.2	V	12	=>	12 T
3rd output	0	V	0	V	0	=>	0 T
4th output	0	V	0	V	0	=>	0 T
5th output	0	V	0	V	0	=>	0 T
6th output	0	V	0	V	0	=>	0 T
VF : Forward voltage drop of rectifier diode			Primary turns =				65 T
			->enough turns				

AL value (no gap)	2130	nH/T^2
Gap length (center pole gap)=	0.41384	mm

7. Determine proper wire for each output

	Diameter		Parallel		Irms		(A/mm^2)
Primary winding	0.5	mm	1	T	1.04	A	5.31
Vcc winding	0.3	mm	1	T	0.10	A	1.42
1st output winding	0.4	mm	4	T	3.73	A	7.41
2nd output winding	0.4	mm	4	T	4.66	A	9.27
3rd output winding	0	mm	0	T	####	A	#DIV/0!
4th output winding	0	mm	0	T	####	A	#DIV/0!
5th output winding	0	mm	0	T	####	A	#DIV/0!
6th output winding	0	mm	0	T	####	A	#DIV/0!

Copper area =	22.0782	mm^2
Fill fator	0.2	
Required window area	110.391	mm^2

Required window area > Aw

(EFD2525 : Aw=77mm^2)

Replace EFD2525 with EFD3030 and

GO Back to Step 5

EFD3030 : Ae=69mm^2, Aw=87mm^2, Ap=6003mm^4

5. Determine proper core and minimum primary turns

Current limit of FPS	2.20	A
Maximum flux density swing	0.35	T
Saturation flux density (Bsat)	0.42	T
Estimated AP value of core =	3929	mm^4
Cross sectional area of core (Ae)	69	mm^2
Minimum primary turns =	51.6	T

6. Determine the numner of turns for each outputs

	Vo		VF			# of turns	
Vcc (Use Vcc start voltage)	12	V	1.2	V	9.6	=>	10 T
1st output for feedback	5	V	0.5	V	4	=>	4 T
2nd output	12	V	1.2	V	9.6	=>	10 T
3rd output	0	V	0	V	0	=>	0 T
4th output	0	V	0	V	0	=>	0 T
5th output	0	V	0	V	0	=>	0 T
6th output	0	V	0	V	0	=>	0 T
VF : Forward voltage drop of rectifier diode			Primary turns =				52 T
			->enough turns				

AL value (no gap)	2130	nH/T^2
Gap length (center pole gap)=	0.30044	mm

7. Determine proper wire for each output

	Diameter		Parallel		Irms		(A/mm^2)
Primary winding	0.5	mm	1	T	1.04	A	5.31
Vcc winding	0.3	mm	1	T	0.10	A	1.42
1st output winding	0.4	mm	4	T	3.73	A	7.41
2nd output winding	0.4	mm	4	T	4.66	A	9.27
3rd output winding	0	mm	0	T	####	A	#DIV/0!
4th output winding	0	mm	0	T	####	A	#DIV/0!
5th output winding	0	mm	0	T	####	A	#DIV/0!
6th output winding	0	mm	0	T	####	A	#DIV/0!
Copper area =	17.8918	mm^2					
Fill factor	0.2						
Required window area	89.459	mm^2					

8. Determine the rectifier diodes in the secondary side

	Reverse voltage		Rms Current	
Vcc diode	82	V	0.10	A
1st output diode	34	V	3.73	A
2nd output diode	82	V	4.66	A
3rd output diode	0	V	####	A
4th output diode	0	V	####	A
5th output diode	0	V	####	A
6th output diode	0	V	####	A

9. Determine the output capacitor

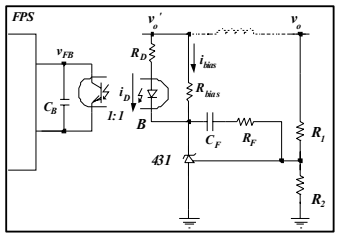
	Capacitance		ESR		Current ripple		Voltage Ripple	
1st output capacitor	1000	uF	30	mΩ	2.8	V	0.21	V
2nd output capacitor	1000	uF	40	mΩ	4.0	V	0.33	V
3rd output capacitor	0	uF	50	mΩ	####	V	####	V
4th output capacitor	0	uF	50	mΩ	####	V	####	V
5th output capacitor	0	uF	50	mΩ	####	V	####	V
6th output capacitor	0	uF	50	mΩ	####	V	####	V

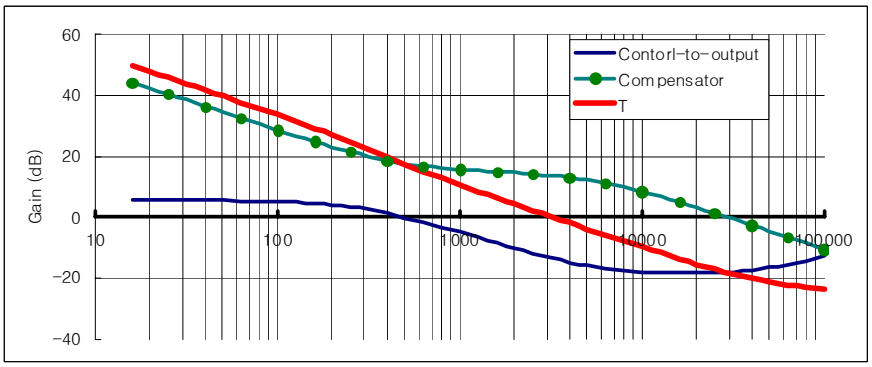
10. Design RCD snubber

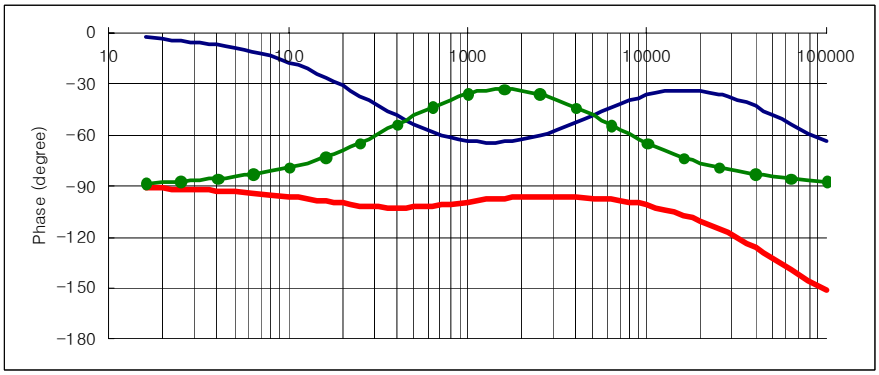
Primary side leakage inductance	4	uH	
Nominal Voltage of snubber capacitor	120	V	
Nominal snubber capacitor voltage rippl	5	%	
Snubber resistor =	27.8821	kΩ	
Snubber capacitor =	10.7061	nF	
Power loss in snubber resistor =	0.51646	W	(In Normal Operation)
Maximum snubber capacitor voltage=	134.474	V	
Maximum MOSFET voltage =	509.24	V	

11. Design Feedback control loop

Control-to-output DC gain =	2	
Control-to-output zero =	5,308	Hz
Control-to-output RHP zero =	54,862	Hz
Control-to-output pole =	306	Hz
Voltage divider resistor (R1)	5.6	kΩ
Voltage divider resistor (R2)	5.6	kΩ
Opto coupler diode resistor (RD)	1	kΩ
431 Bias resistor (Rbias)	1.2	kΩ
Feeback pin capacitor (CB) =	10	nF
Feedback Capacitor (CF) =	33	nF
Feedback resistor (RF) =	4.7	kΩ
Feedback integrator gain (fi) =	2,585	Hz
Feedback zero (fz) =	468.478	Hz
Feedback pole (fp) =	5307.86	Hz







Design Summary

- For the FPS, FSDM0565R is chosen. This device has a fixed switching frequency of 67kHz. Startup and soft-start circuits are implemented inside of the device. It consumes under 1W at 265VAC with 0.5W load with an advanced burst-mode operation
- Since the target system is LCD monitor adaptor, low profile ferrite core (EFD3030) is chosen.
- For output diodes, diodes having rated current more than twice of the actual RMS current are selected due to the limitation of the heat sink size.
- The control bandwidth is 3kHz. Since the crossover frequency is too close the corner frequency of the post filter (additional LC filter), the controller is designed to have enough phase margin of 85 degrees when ignoring the effect of the post filter.
- To limit the current, 10 ohms resistor (R_a) is used in series with the Vcc diode.
- To prevent startup with low input voltage, 56k ohms resistor (Rstr) is used on the startup pin.

Figure 1 shows the final schematic of the flyback converter designed by **FPS Design Assistant.**

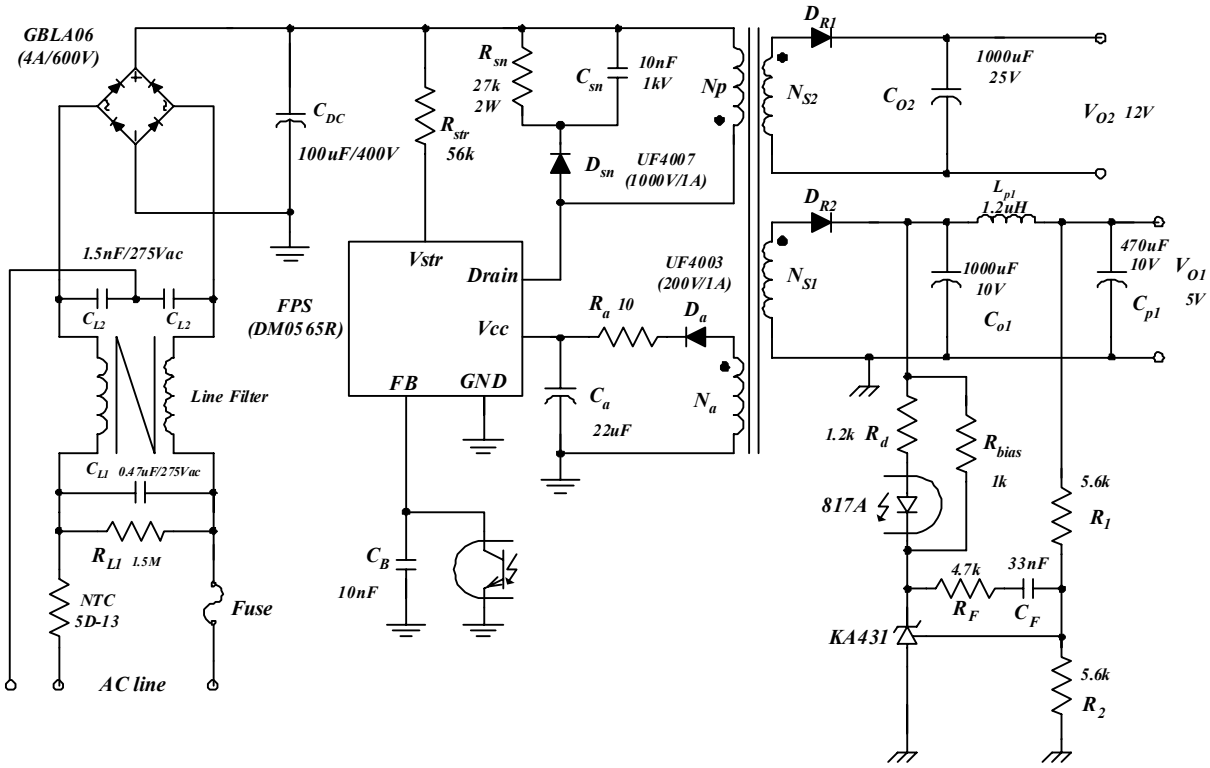


Figure 1. The final schematic of flyback converter

by Hang-Seok Choi / Ph. D

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E-mail : hschoi@fairchildsemi.co.kr

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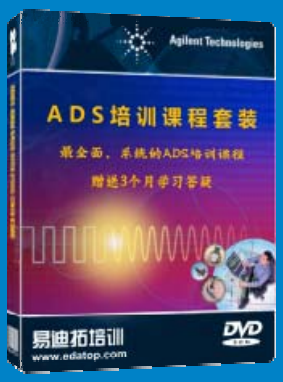

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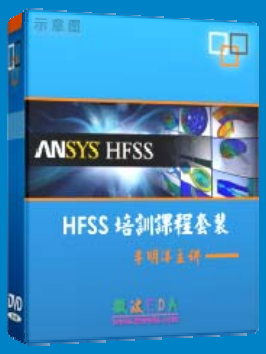

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