Dual SIM/Smart Card Power Supply and Interface

FEATURES

- **Power Management and Control for Two SIM Cards or Smart Cards**
- **Independent 1.8V/3V V_{CC} Control for Both Cards**
- **Supports Simultaneous Powering of Both Cards**
- **Fast Channel Switching**
- **Automatic Level Translation**
- **Dynamic Pull-Ups Deliver Fast Signal Rise Times***
- Built-In Fault Protection Circuitry
- Automatic Activation/Deactivation Sequencing Circuitry
- Low Operating/Shutdown Current
- > 10kV ESD on SIM Card Pins
- Meets EMV Fault Tolerance Requirements
- Low Profile 20-Lead (3mm × 3mm) QFN Package

APPLICATIONS

- GSM, TD-SCDMA and other 3G+ Cellular Phones
- Wireless Point-of-Sale Terminals
- Multiple SIM Card Interfaces

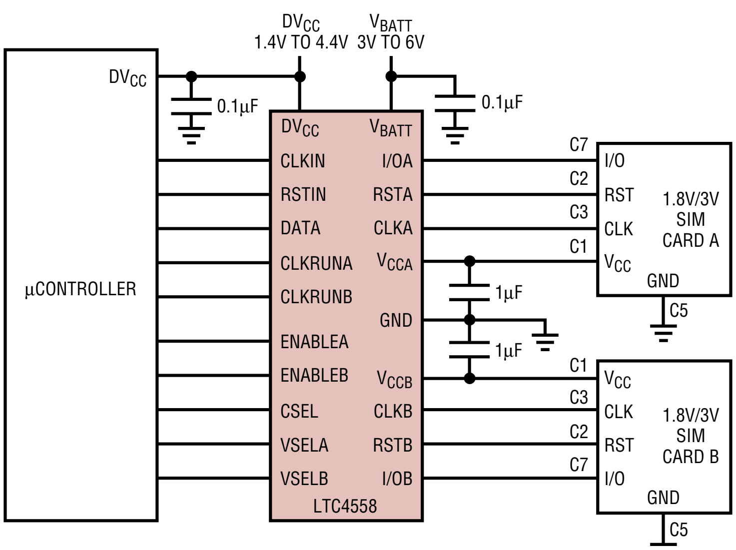
DESCRIPTION

The LTC®4558 provides the power conversion and signal level translation needed for advanced cellular telephones to interface with 1.8V or 3V subscriber identity modules (SIMs). The device meets all requirements for 1.8V and 3V SIMs and contains LDO regulators to power 1.8V or 3V SIM cards from a 2.7V to 5.5V input. The output voltages can be set using the two voltage selection pins and up to 50mA of load current can be supplied. A channel select pin determines which channel is open for communication. Separate enable pins for each channel allow both cards to be powered at once and allow for faster transition from one channel to the other.

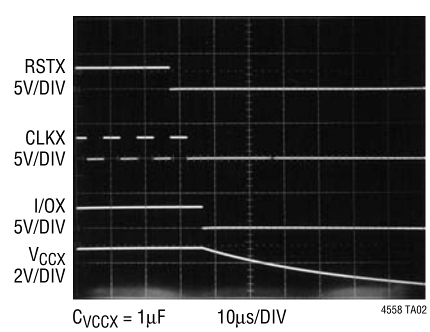
Internal level translators allow controllers operating with supplies as low as 1.4V to interface with 1.8V or 3V Smart Cards. Battery life is maximized by a low operating current of 65μA and a shutdown current of less than 1μA. Board area is minimized by the low profile 3mm × 3mm × 0.75mm leadless QFN package.

*Protected by U.S. Patents, including 6356140.

TYPICAL APPLICATION



Deactivation Sequence



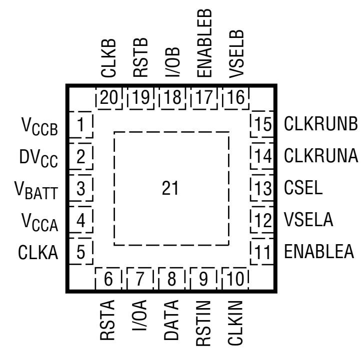
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{BATT}, DV_{CC}, DATA, RSTIN, CLKIN, CLKRUNA, CLKRUNB, ENABLEA, ENABLEB, CSEL, VSELA, VSELB to GND .... −0.3V to 6V
I/OA, CLKA, RSTA .... −0.3V to VCCA + 0.3V
I/OB, CLKB, RSTB .... −0.3V to VCCB + 0.3V
$I_{CCA,B}$ (Note 4) 80mA
$V_{CCA,B}$ Short-Circuit Duration.......................... Indefinite
Operating Temperature Range (Note 3) ...−40°C to 85°C
Storage Temperature Range...................−65°C to 125°C

PACKAGE/ORDER INFORMATION

TOP VIEW



UD PACKAGE
20-LEAD (3mm × 3mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 68°C/W, θ_{JC} = 4.2°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

ORDER PART NUMBER	UD PART MARKING
LTC4558EUD	LCSH

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{BATT} = 3.3V, DV_{CC} = 1.8V, C_A = C_B = 1µF, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Power Supply						
V_{BATT} Operating Voltage		●	2.7		5.5	V
I_{VBATT} Operating Current	V_{CCA} = 3V, V_{CCB} = 0V, I_{CCA} = 0µA V_{CCA} = 1.8V, V_{CCB} = 0V, I_{CCA} = I_{CCB} = 0µA	●		65 65	100 100	µA µA
DV_{CC} Operating Voltage		●	1.4		5.5	V
I_{DVCC} Operating Current		●		6	15	µA
I_{DVCC} Shutdown Current		●		0.1	1	µA
I_{VBATT} Shutdown Current	DV_{CC} = 0V	●		0.1	1	µA
SIM Card Supplies						
$V_{CCA,B}$ Output Voltage	3V Mode, 0mA < $I_{CCA,B}$ < 50mA 1.8V Mode, 0mA < $I_{CCA,B}$ < 30mA	● ●	2.85 1.71	3.00 1.8	3.15 1.89	V V
$V_{CCA,B}$ Turn-On Time	$I_{CCA,B}$ = 0mA, ENABLEA,B ↑ to $V_{CCA,B}$ at 90% Selected Voltage	●		0.8	1.5	ms
Channel Switching Time	ENABLEA = ENABLEB = RSTIN = DV_{CC} CSEL ↑ to RSTB ↑	●		1		µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{BATT} = 3.3V, DV_{CC} = 1.8V, C_A = C_B = 1µF, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CLKA,B						
Low Level Output Voltage (V_{OL})	Sink Current = –200µA (Note 2)	●			0.2	V
High Level Output Voltage (V_{OH})	Source Current = 200µA (Note 2)	●	$V_{CCA,B}$ –0.2			V
Rise/Fall Time	Loaded with 50pF (10% to 90%) (Note 2)	●			16	ns
CLKA,B Frequency	(Note 2)	●	10			MHz
RSTA,B						
Low Level Output Voltage (V_{OL})	Sink Current = –200µA (Note 2)	●			0.2	V
High Level Output Voltage (V_{OH})	Source Current = 200µA (Note 2)	●	$V_{CCA,B}$ –0.2			V
Rise/Fall Time	Loaded with 50pF (10% to 90%) (Note 2)	●			100	ns
I/OA, I/OB						
Low Level Output Voltage (V_{OL})	Sink Current = –1mA (V_{DATA} = 0V) (Note 2)	●			0.3	V
High Level Output Voltage (V_{OH})	Source Current = 20µA (V_{DATA} = V_{DVCC}) (Note 2)	●	0.85 • $V_{CCA,B}$			V
Rise/Fall Time	Loaded with 50pF (10% to 90%) (Note 2)	●			500	ns
Short-Circuit Current	V_{DATA} = 0V (Note 2)	●		5	10	mA
DATA						
Low Level Output Voltage (V_{OL})	Sink Current = –500µA ($V_{I/OA,B}$ = 0V)	●			0.3	V
High Level Output Voltage (V_{OH})	Source Current = 20µA ($V_{I/OA,B}$ = $V_{CCA,B}$)	●	0.8 • DV_{CC}			V
Rise/Fall Time	Loaded with 50pF (10% to 90%)	●		125	500	ns
ENABLEA, ENABLEB, RSTIN, CLKIN, CSEL, VSELA, VSELB, CLKRUNA, CLKRUNB						
Low Input Threshold (V_{IL})		●			0.15 • DV_{CC}	V
High Input Threshold (V_{IH})		●	0.85 • DV_{CC}			V
Input Current (I_{IH}/I_{IL})		●	–1		1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

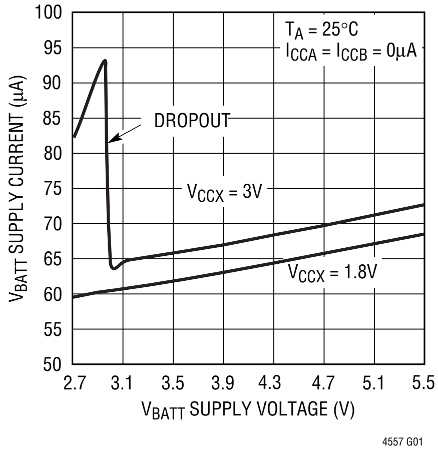
Note 2: This specification applies to both Smart Card classes.

Note 3: The LTC4558E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

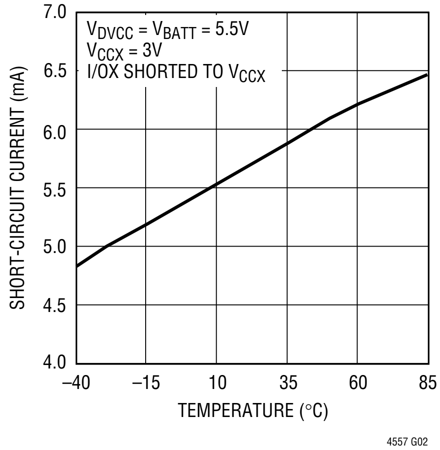
Note 4: Based on long-term current density limitations.

TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$ unless otherwise noted.

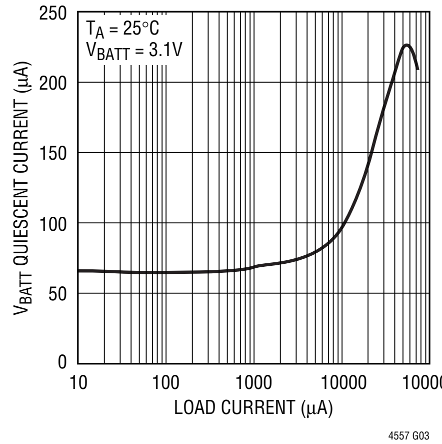
No Load Supply Current vs V_{BATT}



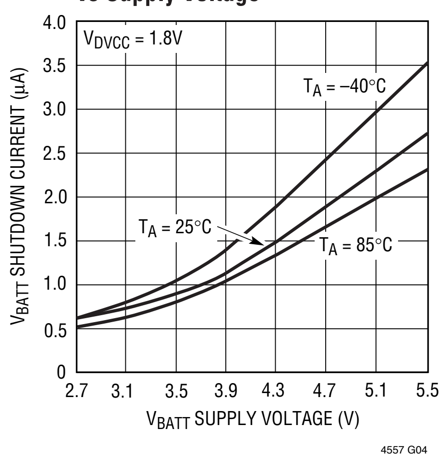
I/OX Short-Circuit Current vs Temperature



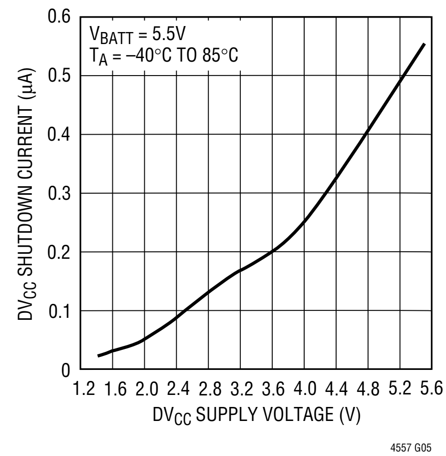
V_{BATT} Quiescent Current ($I_{VBATT} – I_{CC}$) vs Load Current



V_{BATT} Shutdown Current vs Supply Voltage



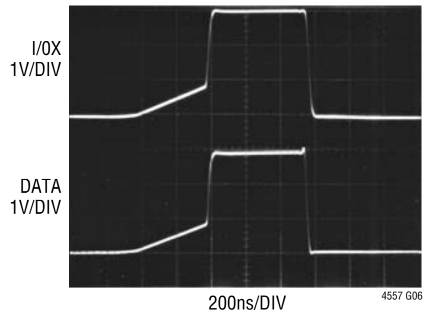
DV_{CC} Shutdown Current vs Supply Voltage



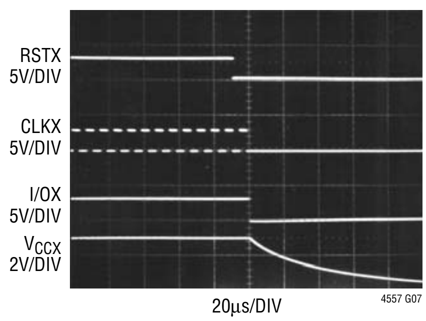
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C unless otherwise noted.

Data – I/O Channel, C_L = 40pF



Deactivation Sequence, C_{VCCX} = 1µF



PIN FUNCTIONS

DV_{CC} (Pin 2): Power. Reference voltage for the control logic.

V_{BATT} (Pin 3): Power. Supply voltage for the analog sections of the LTC4558.

V_{CCA},V_{CCB} (Pins 4, 1): Card Socket. The V_{CCA},V_{CCB} pins should be connected to the V_{CC} pins of the respective card sockets. The activation of the V_{CCA},V_{CCB} pins are controlled by ENABLEA and ENABLEB. They can be set to 1.8V or 3V via the VSELA and VSELB inputs.

CLKA,CKLB (Pins 5, 20): Card Socket. The CLKA,CKLB pins should be connected to the CLK pins of the respective card sockets. The CLKA,CKLB signals are derived from the CLKIN pin. They provide a level shifted CLKIN signal to the selected card. The CLKA,CKLB pins are gated off until V_{CCA},V_{CCB} attain their correct values. When a card socket is deselected, its CLK pin may be left active or brought LOW using the CLKRUNA, CLKRUNB pins.

RSTA,RSTB (Pins 6, 19): Card Socket. The RSTA,RSTB pins should be connected to the RST pins of the respective card sockets. The RSTA,RSTB signals are derived from the RSTIN pin. When a card is selected, its RST pin follows RSTIN. The RSTA,RSTB pins are gated off until V_{CCA},V_{CCB} attain their correct values. When a card socket is deselected, the state of its RST pin is latched to its current state.

I/OA,I/OB (Pins 7, 18): Card Socket. The I/OA,I/OB pins should be connected to the I/O pins of the respective card sockets. When a card is selected, its I/O pin transmits/receives data to/from the DATA pin. The I/OA,I/OB pins are gated off until V_{CCA},V_{CCB} attain their correct values.

DATA (Pin 8): Input/Output. Microcontroller side data I/O pin. The DATA pin provides the bidirectional communication path to both cards. One of the cards may be selected to communicate via the DATA pin at a time. The pin possesses a weak pull-up current source, allowing the controller to use an open drain output and maintain a HIGH state during shutdown, as long as DV_{CC} is powered.

RSTIN (Pin 9): Input. The RSTIN pin supplies the reset signal to the cards. It is level shifted and transmitted directly to the RST pin of the selected card.

CLKIN (Pin 10): Input. The CLKIN pin supplies the clock signal to the cards. It is level shifted and transmitted directly to the CLK pin of the selected card. If CLKRUNA,B is HIGH, the clock signal will be transmitted to the CLKA,B pin, regardless of whether that card is selected, as long as that card socket is enabled.

ENABLEA, ENABLEB (Pins 11, 17): Inputs. The ENABLEA and ENABLEB pins enable or disable channel A and channel B, respectively.

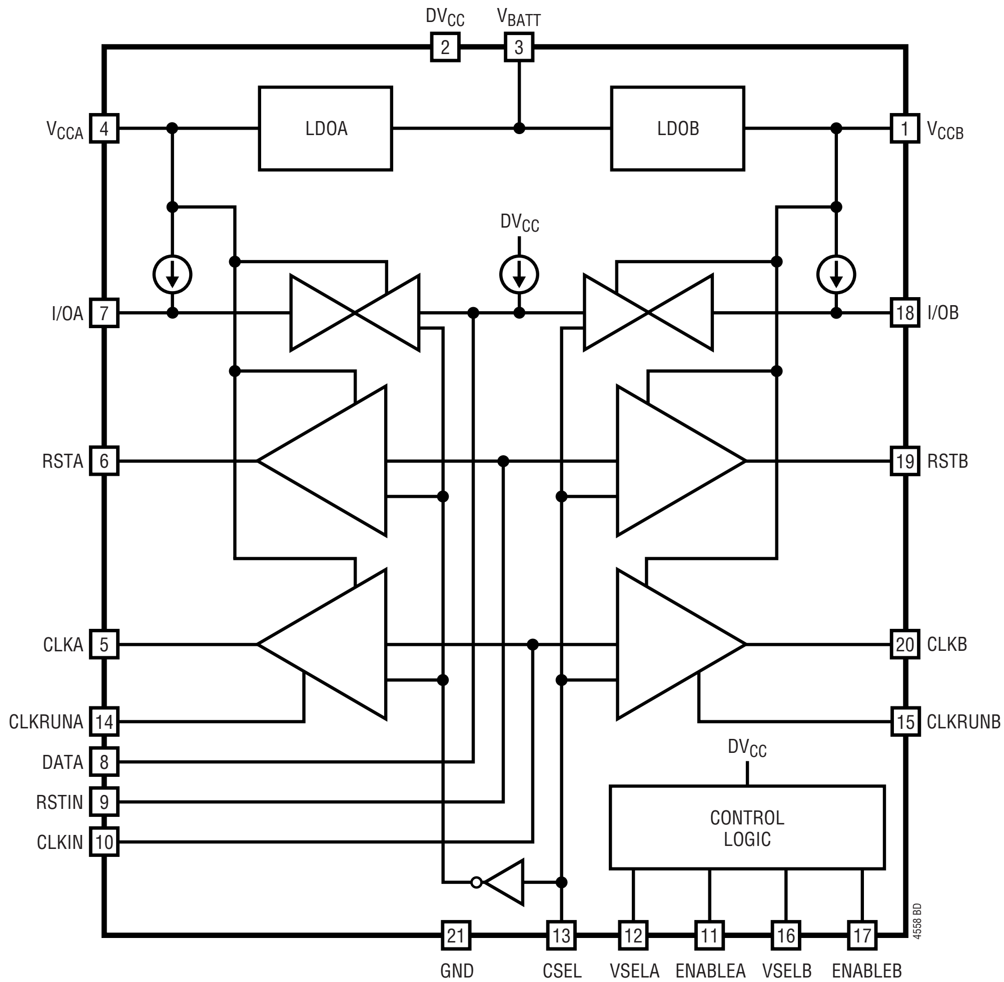
VSELA, VSELB (Pins 12, 16): Inputs. The VSELA and VSELB pins select the voltage level of each set of SIM/Smart Card pins. Bringing either of these pins HIGH will set the output level of its respective channel to 3V. Bringing either of these pins LOW will set the output level of its respective channel to 1.8V.

CSEL (Pin 13): Input. The CSEL pin selects which set of SIM/Smart Card pins are active.

CLKRUNA, CLKRUNB (Pins 14, 15): Inputs. The CLKRUNA and CLKRUNB inputs are used to select whether the clock signal is always sent to card sockets that are enabled or whether the clock is gated with the CSEL pin.

Exposed Pad (Pin 21): Ground. This ground pad must be soldered directly to a PCB ground plane.

BLOCK DIAGRAM



OPERATION

The LTC4558 features two independent SIM/Smart Card channels. Only one of these channels may be open for communication at a time however both channels can be enabled and made ready for communication using the ENABLEA and ENABLEB pins. This allows faster transition from one channel to the other. Each channel is able to produce two voltage levels, 1.8V and 3V. The channel selection and voltage selection are controlled by the CSEL, VSELA and VSELB pins as shown in the table below:

Table 1. Channel and Voltage Truth Table

CSEL	VSELA	VSELB	SELECTED CARD	VOLTAGES A	VOLTAGES B
0	0	0	A	1.8V	1.8V
0	0	1	A	1.8V	3V
0	1	0	A	3V	1.8V
0	1	1	A	3V	3V
1	0	0	B	1.8V	1.8V
1	0	1	B	1.8V	3V
1	1	0	B	3V	1.8V
1	1	1	B	3V	3V

Bidirectional Channels

The bidirectional channels are level shifted to the appropriate $V_{CCA,B}$ voltages at the I/OA,B pins. An NMOS pass transistor performs the level shifting. The gate of the NMOS transistor is biased such that the transistor is completely off when both sides have relinquished the channel. If one side of the channel asserts a LOW, then the transistor will convey the LOW to the other side. Note that current passes from the receiving side of the channel to the transmitting side. The low output voltage of the receiving side will be dependent upon the voltage at the transmitting side plus the IR drop of the pass transistor.

When a card socket is selected, it becomes a candidate to drive data on the DATA pin and likewise receive data from the DATA pin. When a card socket is deselected, its I/O pin will be pulled HIGH and communication with the DATA pin will be disabled. If both channels are disabled, a weak pull-up ensures that the DATA pin is held HIGH, as long as DV_{CC} is powered.

Dynamic Pull-Up Current Sources

The current sources on the bidirectional pins (DATA,I/OA,B) are dynamically activated to achieve a fast rise time with a relatively small static current. Once a bidirectional pin is relinquished, a small start-up current begins to charge the node. An edge rate detector determines if the pin is released by comparing its slew rate with an internal reference value. If a valid transition is detected, a large pull-up current enhances the edge rate on the node. The higher slew rate corroborates the decision to charge the node thereby affecting a dynamic form of hysteresis.

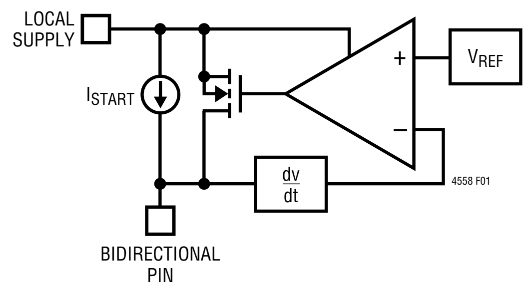


Figure 1. Dynamic Pull-Up Current Source

Reset Channels

When a card is selected, the reset channel provides a level shifted path from the RSTIN pin to the RST pin of the selected card. When a card is deselected, the last state of the RSTA,B pin is latched. This allows a deselected card to remain active, and therefore eliminates delays associated with card initialization.

Clock Run Mode

Various SIM/Smart Cards may have different requirements for the state of the clock pin when the channel is not open for communication. The CLKRUNA,B pins allow the user to select whether the clock is brought LOW after the channel is deselected or allowed to run. If a channel is enabled, bringing its CLKRUN pin HIGH will transmit the clock to the corresponding card socket, whether or not the channel is selected using the CSEL.

OPERATION

Activation/Deactivation

Activation and deactivation sequencing is handled by built-in circuitry. Each channel may be activated or deactivated independently of the other. The activation sequence for each channel is initiated by bringing the ENABLEA,B pin HIGH. The activation sequence is outlined below:

1. The RSTA,B, CLKA,B and I/OA,B pins are held LOW.
2. $V_{CCA,B}$ is enabled.
3. After $V_{CCA,B}$ is stable at its selected level, the I/OA,B and RSTA,B channels are enabled.
4. The clock channel is enabled on the rising edge of the second clock cycle after the I/OA,B pin is enabled.

The deactivation sequence is initiated by bringing the ENABLEA,B pin LOW. The deactivation sequence is outlined below:

1. The reset channel is disabled and RSTA,B is brought LOW.
2. The clock channel is disabled and the CLKA,B pin is brought LOW two clock cycles after ENABLEA,B is brought LOW. If the clock is not running, the clock channel will be disabled approximately 9µs after the ENABLEA,B pin is brought LOW.
3. The I/O channel is disabled and the I/OA,B pin is brought LOW approximately 9µs after the ENABLEA,B pin is brought LOW.
4. $V_{CCA,B}$ will be depowered after the I/OA,B pin is brought LOW.

The activation or deactivation sequences will take place every time a card channel is enabled or disabled. When a channel is deselected using the CSEL pin, the RSTA,B state is latched, the I/OA,B channel becomes high impedance and CLKA,B is brought LOW after a maximum of two clock cycles.

Fault Detection

The $V_{CCA,B}$, I/OA,B, RSTA,B, CLKA,B and DATA pins are all protected against short-circuit faults. While there are no logic outputs to indicate that a fault has occurred, these pins will be able to tolerate the fault condition until it has been removed.

The $V_{CCA,B}$, I/OA,B, and RSTA,B pins possess fault protection circuitry which will limit the current available to the pins. Each V_{CC} pin is capable of supplying approximately 90mA (typ) before the output voltage is reduced.

The CLKA,B pins are designed to tolerate faults by reducing the current drive capability of their output stages. After a fault is detected by the internal fault detection logic, the logic waits for a fault detection delay to elapse before reducing the current drive capability of the output stage. The reduced current drive allows the LTC4558 to detect when the fault has been removed.

APPLICATIONS INFORMATION

10kV ESD Protection

All Smart Card pins (CLKA,B, RSTA,B, I/OA,B, $V_{CCA,B}$ and GND) can withstand over 10kV of human body model ESD in-situ. In order to ensure proper ESD protection, careful board layout is required. The GND pin should be tied directly to a ground plane. The $V_{CCA,B}$ capacitors should be located very close to the $V_{CCA,B}$ pins and tied immediately to the ground plane.

Capacitor Selection

A total of four capacitors is required to operate the LTC4558. An input bypass capacitor is required at V_{BATT} and DV_{CC}. Output bypass capacitors are required on each of the Smart Card V_{CC} pins.

There are several types of ceramic capacitors available, each having considerably different characteristics. For example, X7R ceramic capacitors have excellent voltage and temperature stability but relatively low packing density. Y5V and X5R ceramic capacitors have apparently higher packing density but poor performance over their rated voltage or temperature ranges. Under certain voltage and temperature conditions Y5V, X5R and X7R ceramic capacitors can be compared directly by case size rather than specified value for a desired minimum capacitance.

The $V_{CCA,B}$ outputs should be bypassed to GND with a 1µF capacitor. A low ESR ceramic capacitor is recommended on each V_{CC} pin to ensure ESD compliance.

V_{BATT} and DV_{CC} should be bypassed with 0.1µF ceramic capacitors.

Compliance Testing

Inductance due to long leads on type approval equipment can cause ringing and overshoot that leads to testing problems. Small amounts of capacitance and damping resistors can be included in the application without compromising the normal electrical performance of the LTC4558 or Smart Card system. Generally a 100Ω resistor and a 20pF capacitor will accomplish this, as shown in Figure 2.

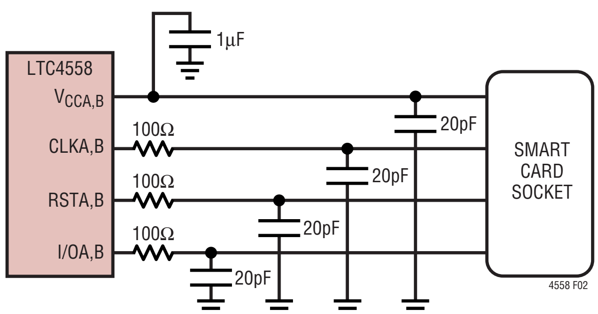
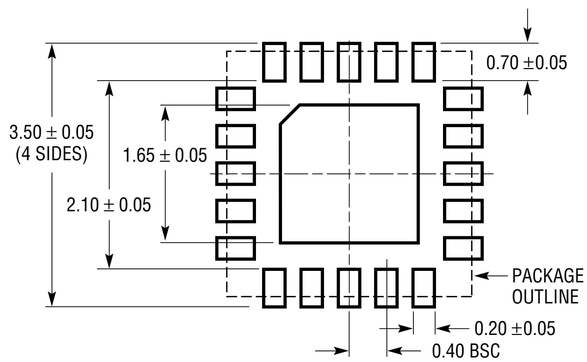


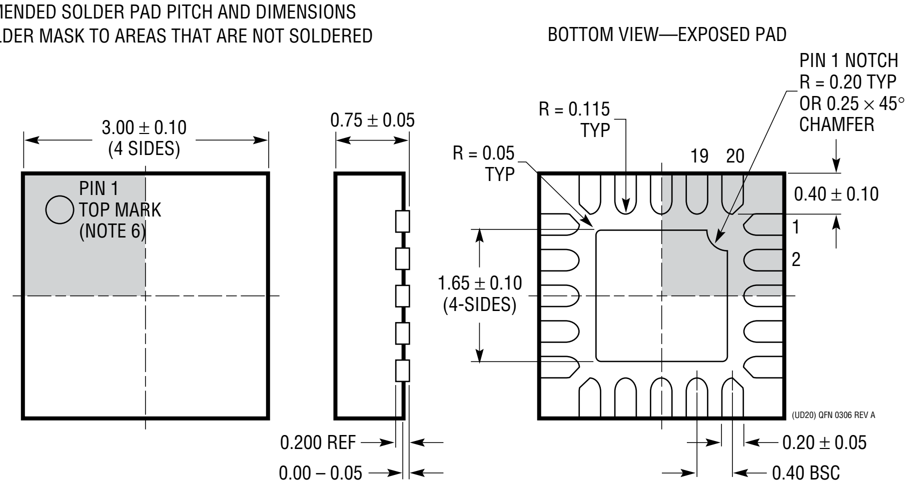
Figure 2. Additional Components for Improved Compliance Testing

PACKAGE DESCRIPTION

UD Package
20-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1720 Rev A)

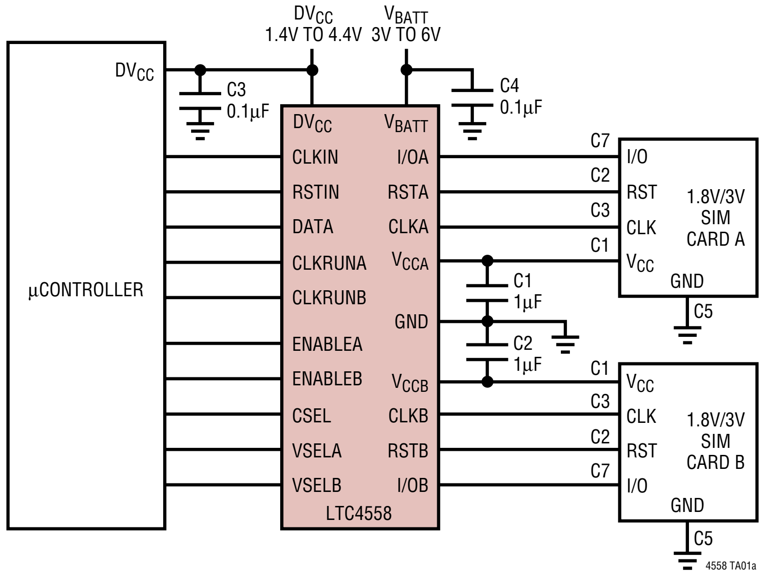


RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1555L/ LTC1555L-1.8	1MHz, SIM Power Supply and Level Translator for 1.8V/3V/5V SIM Cards	V_{IN}: 2.6V to 6.6V, V_{OUT} = 1.8V/3V/5V, I_Q = 32µA, I_{SD} < 1µA, SSOP16
LTC1555/LTC1556	650kHz, SIM Power Supply and Level Translator for 3V/5V SIM Cards	V_{IN}: 2.7V to 10V, V_{OUT} = 3V/5V, I_Q = 60µA, I_{SD} < 1µA, SSOP16, SSOP20
LTC1755/LTC1756	850kHz, Smart Card Interface with Serial Control for 3V/5V Smart Card Applications	V_{IN}: 2.7V to 7V, V_{OUT} = 3V/5V, I_Q = 60µA, I_{SD} < 1µA, SSOP16, SSOP24
LTC1955	Dual Smart Card Interface with Serial Control for 1.8V/3V/5V Smart Card Applications	V_{IN}: 3V to 5.5V, V_{OUT} = 1.8V/3V/5V, I_Q = 200µA, I_{SD} < 1µA, QFN32
LTC1986	900kHz, SIM Power Supply for 3V/5V SIM Cards	V_{IN}: 2.6V to 4.4V, V_{OUT} = 3V/5V, I_Q = 14µA, I_{SD} < 1µA, ThinSOT
LTC4555	SIM Power Supply and Level Translator for 1.8V/3V SIM Cards	V_{IN}: 3V to 6V, V_{OUT} = 1.8V/3V, I_Q = 40µA, I_{SD} < 1µA, QFN16
LTC4556	Smart Card Interface with Serial Control	V_{IN}: 2.7V to 5.5V, V_{OUT} = 1.8V/3V/5V, I_Q = 250µA, I_{SD} < 1µA, 4 × 4 QFN24
LTC4557	Dual SIM/Smart Card Power Supply and Level Translator for 1.8V/3V Cards	V_{IN}: 2.7V to 5.5V, V_{OUT} = 1.8V/3V, I_Q = 250µA, I_{SD} < 1µA, QFN16

ThinSOT is a trademark of Linear Technology Corporation.

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射 频 和 天 线 设 计 培 训 课 程 推 荐

易迪拓培训(www.edatop.com)由数名来自于研发第一线的资深工程师发起成立，致力并专注于微波、射频、天线设计研发人才的培养；我们于 2006 年整合合并微波 EDA 网(www.mweda.com)，现已发展成为国内最大的微波射频和天线设计人才培养基地，成功推出多套微波射频以及天线设计经典培训课程和 ADS、HFSS 等专业软件使用培训课程，广受客户好评；并先后与人民邮电出版社、电子工业出版社合作出版了多本专业图书，帮助数万名工程师提升了专业技术能力。客户遍布中兴通讯、研通高频、埃威航电、国人通信等多家国内知名公司，以及台湾工业技术研究院、永业科技、全一电子等多家台湾地区企业。

易迪拓培训课程列表：http://www.edatop.com/peixun/rfe/129.html

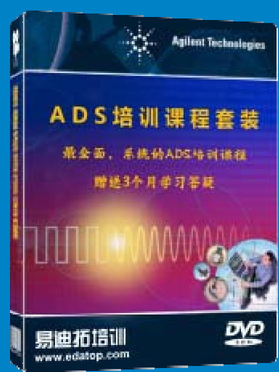
射频工程师养成培训课程套装

该套装精选了射频专业基础培训课程、射频仿真设计培训课程和射频电路测量培训课程三个类别共 30 门视频培训课程和 3 本图书教材；旨在引领学员全面学习一个射频工程师需要熟悉、理解和掌握的专业知识和研发设计能力。通过套装的学习，能够让学员完全达到和胜任一个合格的射频工程师的要求…

课程网址：http://www.edatop.com/peixun/rfe/110.html

ADS 学习培训课程套装

该套装是迄今国内最全面、最权威的 ADS 培训教程，共包含 10 门 ADS 学习培训课程。课程是由具有多年 ADS 使用经验的微波射频与通信系统设计领域资深专家讲解，并多结合设计实例，由浅入深、详细而又全面地讲解了 ADS 在微波射频电路设计、通信系统设计和电磁仿真设计方面的内容。能让您在最短的时间内学会使用 ADS，迅速提升个人技术能力，把 ADS 真正应用到实际研发工作中去，成为 ADS 设计专家...



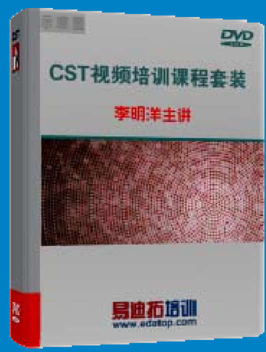
课程网址： http://www.edatop.com/peixun/ads/13.html

HFSS 学习培训课程套装

该套课程套装包含了本站全部 HFSS 培训课程，是迄今国内最全面、最专业的HFSS培训教程套装，可以帮助您从零开始，全面深入学习HFSS的各项功能和在多个方面的工程应用。购买套装，更可超值赠送 3 个月免费学习答疑，随时解答您学习过程中遇到的棘手问题，让您的 HFSS 学习更加轻松顺畅…

课程网址：http://www.edatop.com/peixun/hfss/11.html

CST 学习培训课程套装



该培训套装由易迪拓培训联合微波 EDA 网共同推出，是最全面、系统、专业的 CST 微波工作室培训课程套装，所有课程都由经验丰富的专家授课，视频教学，可以帮助您从零开始，全面系统地学习 CST 微波工作的各项功能及其在微波射频、天线设计等领域的设计应用。且购买该套装，还可超值赠送 3 个月免费学习答疑…

课程网址：http://www.edatop.com/peixun/cst/24.html

HFSS 天线设计培训课程套装

套装包含 6 门视频课程和 1 本图书，课程从基础讲起，内容由浅入深，理论介绍和实际操作讲解相结合，全面系统的讲解了 HFSS 天线设计的全过程。是国内最全面、最专业的 HFSS 天线设计课程，可以帮助您快速学习掌握如何使用 HFSS 设计天线，让天线设计不再难…

课程网址：http://www.edatop.com/peixun/hfss/122.html

13.56MHz NFC/RFID 线圈天线设计培训课程套装

套装包含 4 门视频培训课程，培训将 13.56MHz 线圈天线设计原理和仿真设计实践相结合，全面系统地讲解了 13.56MHz 线圈天线的工作原理、设计方法、设计考量以及使用 HFSS 和 CST 仿真分析线圈天线的具体操作，同时还介绍了 13.56MHz 线圈天线匹配电路的设计和调试。通过该套课程的学习，可以帮助您快速学习掌握 13.56MHz 线圈天线及其匹配电路的原理、设计和调试…

详情浏览：http://www.edatop.com/peixun/antenna/116.html

我们的课程优势：

※ 成立于 2004 年，10 多年丰富的行业经验，

※ 一直致力并专注于微波射频和天线设计工程师的培养，更了解该行业对人才的要求

※ 经验丰富的一线资深工程师讲授，结合实际工程案例，直观、实用、易学

联系我们：

※ 易迪拓培训官网：http://www.edatop.com

※ 微波 EDA 网：http://www.mweda.com

※ 官方淘宝店：http://shop36920890.taobao.com