EMC on Chip-Level – A New Challenge?

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Abstract:

Advances in device technology are progressing at such a rate that the functionality of integrated circuits (ICs) nearly doubles every year. The evolution of device technology has yielded devices with clock rates in the GHz range and rise/fall times in the order of a few pico seconds. Without a proper design, these high speeds often result in high radiated and conducted emissions. The customer can no longer assume that the system in which modern ICs are implemented will meet the compulsory limits and performance compatibility with other electronic systems. Generally speaking, electromagnetic compatibility (EMC) is defined as the ability of an electrical system to work properly in its electromagnetic environment without unduly interfering with this environment. This is the reason why EMC is of importance to all of us. Consider, for example, the omnipresent electromagnetic environment in our motor vehicles generated by devices like ABS braking systems, airbag sensors, or motor management systems. EMC of ICs has become a limiting factor in the performance of many advanced electronic systems. Therefore, research became necessary in this field to understand the way in which emissions of ICs are generated and what can be done to improve their susceptibility.

1 The role of EMC for the microelectronics industry

The electromagnetic compatibility of integrated circuits has permanently gained more and more significance during the last years. A high level of unwanted emission may cause serious degradations of EMC features of the electronic application in which ICs are used. Therefore, the manufacturers of electronic devices and systems are forced to develop their products according to EMC requirements. However, the semiconductor manufacturers also will have to consider electromagnetic emissions and susceptibility of their products. In the past, the major concerns of the semiconductor industry were cost, area, performance, and reliability; EMC was mostly of no or secondary importance.

Today, the EMC of ICs has emerged as a principal theme. The need for low emission of electromagnetic energy as well as a high-level of susceptibility against it has caused EMC to be as important as performance and functionality.

Although, an IC usually does not radiate significantly, the IC is often seen as the source of overall radiated energy of the electronic systems. Many problems originate from the fact that most of the digital signals are switched as fast as possible, resulting in an increasing amount of high frequency spectral content.

Figure 1 shows these technology trends by means of ASICs. As can be seen the operating frequency, as well as the number of transistors being integrated on a die, has increased remarkably during the last years. On the other hand, the supply voltage and the channel length of the transistors has decreased in order to be able to handle problems caused by size and power dissipation, which for example makes ICs more vulnerable. In general, ICs are extremely susceptible to radio frequency (RF) signals and may react in an unwanted manner to demodulated signals. This often causes failures of the designed function and may be safety critical.

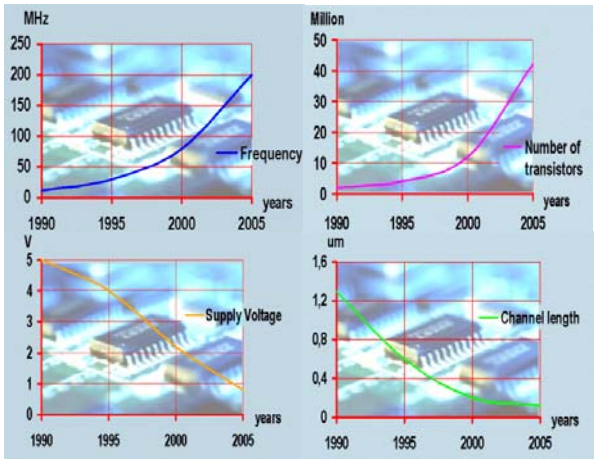

Figure 1: Technology trend (ASICs).

For this reason, implementing EMC measures on chip-level is absolutely necessary to meet today's demands.

Especially for automotive applications, EMC characterization on chip-level became a significant attribute of quality and thus a decisive criterion for a customer's choice of components.

Today's improvements concerning chip-level performance, speed, and technology sound fabulous. However, problems become evident when you imagine the consequence of agglomerating many chips into a system-level product. The emission of electromagnetic energy is increasing at an exponential rate, whereas the susceptibility is decreasing.

Mathematically, unless the EMC performance can increase along the same exponential pace as the ICs improvements, the EMC will eventually become a serious impediment to overall system performance. That is happening right now.

This does not mean that all the EMC experts have been resting on their laurels, but in fact we can count on the fingers of one hand the number of big, widespread advances in EMC on chip-level in the last years. With placing the VDD and GND pins close to each other, implementing on-chip decoupling, controlling the slew rate, making analog parts more robust being some of the prominent advances. So far, these advances were sufficient to keep up with the chip industry, but in the future further progress will be necessary.

To fully realize the benefits of advanced ICs, here is what will be required:

Better knowledge of how the ground bounce and consequently common mode currents affect the electromagnetic emissions, better package models for simulation, better tools for EMC management on chip-level, reduction of signal-integrity problems, higher susceptibility of analog building- and I/O-blocks to RF interference, better control over radiated emissions, better packages with less parasitic elements, advanced control of the rise and fall times of the output signals (moderate slew rate), and of course more design engineers who understand the generation of ICs emissions.

If we follow all these points, we can expect to keep up with Moore's Law for a long time.

2 Characterizing the EMC on chip –level

However, as EMC characterization on chip-level is a relatively new subject, well-defined standards and emission reference levels already exist for electronic systems and subsystems, but not yet for the ICs used within these systems. Accepted EMC measurement procedures on chip-level will close that gap [i], [ii].

The subcommittee 47A (Integrated Circuits) of the IEC[1] is just working on two standards for the characterization of the EMC of integrated circuits. In the near future, we will be able to characterize the electromagnetic emission of ICs according to the IEC 61967 standard and the immunity of ICs according to the IEC 62132 standard. Although the measurement methods described in these two standards will never be able to completely eliminate EMC measurements on system-level, a design engineer will have the ability to identify the main sources of the emissions and the parts having the weakest susceptibility in his application.

At present the "IEC 61967: Integrated circuits – Measurement of electromagnetic emissions 150kHz to 1GHz" standard consists of six parts:

Part 1: General conditions and definitions

Part 2: Measurement of radiated emissions – TEM-cell method

Part 3: Measurement of radiated emissions – Surface scan method

Part 4: Measurement of conducted emissions – 1Ω/150Ω direct coupling method

Part 5: Measurement of conducted emissions – Workbench Faraday cage method

Part 6: Measurement of conducted emissions – Magnetic probe method

The second standard "IEC 62132: Integrated circuits - Measurement of electromagnetic immunity" currently consists of 5 parts.

Part 1: General conditions and definitions

Part 2: Measurement of radiated immunity – TEM cell method

Part 3: Measurement of conducted immunity – Bulk current injection method (BCI)

Part 4: Measurement of conducted immunity – Direct power injection method (DPI)

Part 5: Measurement of conducted immunity – Workbench Faraday Cage method

All the measuring methods, which are described in these two standards, can be used as a basis for the specification of the emission and the immunity of integrated circuits. All these methods have their advantages and limitations. Therefore, the designer of electronic applications, as well as the semiconductor manufacturer, should carefully select those measuring methods, which best fits their requirements. Although we are able to characterize the EMC of ICs on chip-level using these measuring methods, it will not be possible to directly compare between system- and chip-

[1] The IEC (International Electrotechnical Commission) is a worldwide organization for standardization comprising all national electrotechnical committees. The object of the IEC is to promote international cooperation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities the IEC publishes International Standards.

level measurements. The manufacturer of electronic applications will always have to perform EMC measurements of the whole system, even if the IC has passed the EMC requirements on chip-level.

Often, the typical EMC measures, like filters or shielding techniques are necessary to fulfil the EMC requirements of the electronic application. Where those EMC measures are realized (within the IC or for example on the PCB) depends on cost aspects and feasibility considerations (space availability, etc.).

The most effective way of solving EMC problems is to pinpoint and reduce the actual sources of the interference. A very important method to tackle EMC problems already on chip-level is the so-called "surface scan method (IEC 61967-3)". With this method the actual magnetic components, as well as the electric components of the electromagnetic field at the surface of the IC can be visualized. Using this method, the source of the electromagnetic emission of an IC can be located very easily.

3 IEC 61967-3: The surface scan method

This part of the IEC 61967 standard describes a method for evaluating the near electric (E) field or the near magnetic (H) field component at the surface of an IC [iii]. This method can be used over the frequency range from 10MHz to 3GHz. To measure the distribution of these fields an E- or an H-field probe is mechanically moved over the surface of the IC, where the probe can be placed in a parallel or perpendicular plane to the IC surface. The measured data can be computer processed and the field strength at a specific scan frequency can be visualized in a colored representation. The resolution reachable with this method is closely linked to the precision of the mechanical probe positioning system and the size of the used probes. In addition, comparisons between different design steps can be done in order to show improvements in the design. This measurement method can be applied to any IC mounted on a printed circuit board (PCB) that is accessible to the probe. For comparison measurements between different chip architectures, a standardized test board shall be used, which is described in [iv]. The electric and magnetic field scan over the surface of the IC yields information of the relative strength of the sources of the electromagnetic emission (EME). This method provides a useful tool to spot areas on the die with an excessive EME within the IC package.

4 E- and H-field Probes

To measure the electric field, the mechanical design of a micro sized E-field probe, which usually has a partial shield, is suggested in the IEC 61967-3 standard. For H-field measurements, this standard recommends the use of a single turn micro sized H-field probe; either stand-alone or generated as a PCB trace. Both probes can be fabricated from a 0.020 inch semi-rigid coaxial cable. The typical effective aperture of the H-filed probe is about 200 micrometers. Figure 2 shows an example of an E- and an H-field probe built by a coaxial cable.

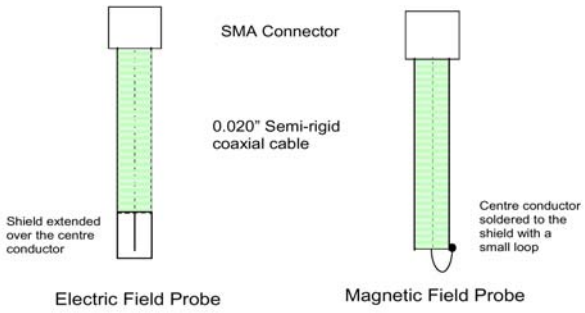

Figure 2: E and H near-field probes.

A practical implementation of an H-field probe can be seen in Figure 3. In addition to the shield of the coax-cable a second shield has been applied to improve the shielding of the probe.

Figure 3: H-field probe.

5 Surface scan, practical implementation

In the laboratory of austriamicrosystems AG, the probes are moved by a micropositioner with three linear stages (see Figure 4). To scan a rectangular area on the surface of an IC and to computer process the measured data, a Labview-program has been developed to move the probe in a perpendicular pattern over the surface of the IC.

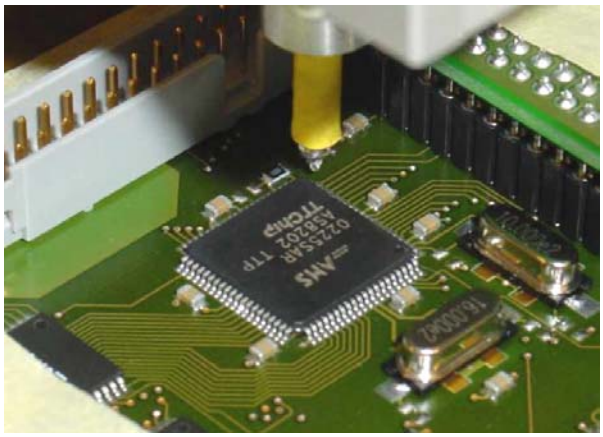

Figure 4: Surface scan setup (IC with H-field probe).

This program controls the XYZ-Scan desk and sets the parameters of the spectrum analyzer, which is used to measure the spectrum of the output voltage of the electric or magnetic field probe. The probe is moved over a defined area above the surface of the IC and captures the measured frequency spectrum from the spectrum analyzer at every measurement point. The program provides a 2D-graph of the measured magnetic or electric field. For further processing, the measured data can be saved to an ASCII-File (for example this file can be imported into Matlab in order to obtain a 3D plot). The step size for a scan over a die should be typically 80 micrometers whereas a step size of 300 micrometers is used to scan the whole IC package. The minimum scan step size depends on the size of the chip and of course on the precision of the positioning system.

The probe can also be placed individually at any position over the die or the IC package. This allows measurements of the electromagnetic emissions directly over a specific part of the die, for example over a high-speed operational amplifier.

6 Measurement of the magnetic field over a package

The magnetic field scan over the IC-package is shown in Figure 5. This picture clearly illustrates areas (bond wire, lead frame) having higher magnetic field components. In this case, these areas are figured out to be the digital I/O and the clock lines. Very often the pins with higher magnetic emission are power supply pins and loaded output pins of the IC, due to the high crowbar currents in combination with the high dynamic switching currents. As these pins are responsible for the overall electromagnetic emission of the IC, EMC measures should be applied here.

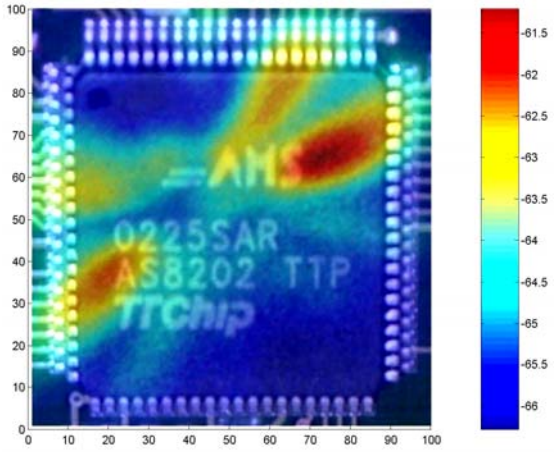

Figure 5: Magnetic field at the surface of an IC package.

A 3D plot of the measurement results can be used as a more precise way to illustrate the magnetic field components over the scanned area (Figure 6).

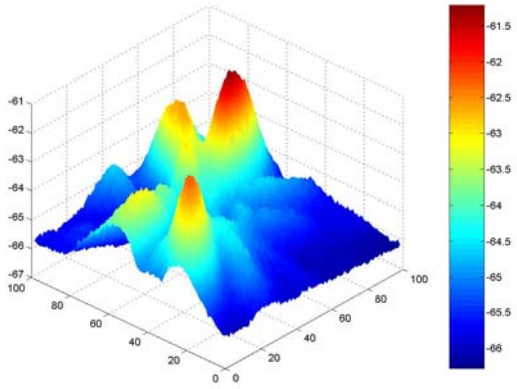

Figure 6: 3D plot of the magnetic field.

7 Measurement of magnetic fields over a die

To measure the spread of the magnetic field over a die, a very small H-field probe has to be used. We are using an H-field probe having two windings of insulated copper wire with an aperture of about 100 micrometers soldered to a piece of coax cable.

A spread of the magnetic field over the die is illustrated in Figure 7. The aim of the surface scan over a die is to exactly localize areas of high unwanted electromagnetic energy. We can see that the resolution of the distribution of the magnetic field is good enough to directly pinpoint specific areas on the die which are responsible for the electromagnetic emissions. The areas of higher magnetic fields are again highlighted in red and the areas having lower magnetic fields are shown in blue. With the knowledge of the location of areas having higher magnetic fields, the designer is able to redesign his circuit in order to reduce the

overall electromagnetic emissions. Also the layout engineer is given hints how to place the parts for lower emissions.

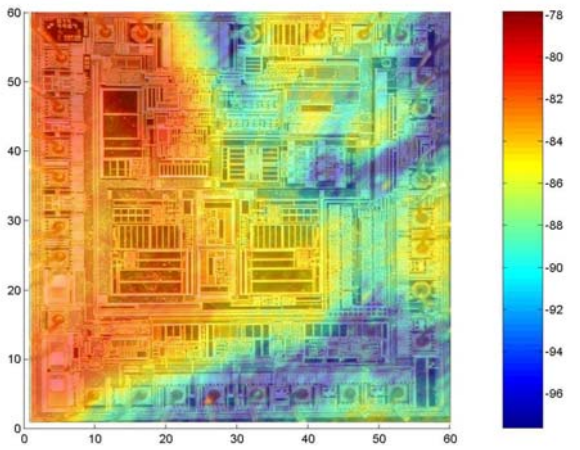

Figure 7: Magnetic field at the surface of a die.

Conclusion

The characterization of the electromagnetic compatibility of integrated circuits has become a very important theme for the microelectronics industry. In fact, without the knowledge of the electromagnetic emission and the immunity of integrated circuits, it is extremely difficult to meet the EMC requirements of electronic applications. As the operating frequencies and the chip complexity continue to grow, the design of ICs having low electromagnetic emissions and a high level of immunity will more and more continue to turn into a very challenging issue. In the future, it seems that every semiconductor manufacturer will have to characterize the electromagnetic emissions and the immunity of their integrated circuits by using the different measurement methods, which are described in the new standards (IEC 61967 and IEC 62132). One of these measurement methods, the so-called "Surface Scan Method" (IEC 61967-3), can easily be used to pinpoint the main sources contributing to the overall electromagnetic emission.

About the Author:

Dr. Bernd Deutschmann has received his M.Sc. degree and the Ph.D. degree in telecommunication engineering from the University of Technology Graz, Austria, in 1999 and 2002, respectively. His doctoral research dealt with the improvement of the electromagnetic compatibility of integrated circuits. He joined the electronic and safety technology group at the Austrian Research Centers Seibersdorf in 1999, where he was responsible for the design and development of hardware systems for an information technology project.

In August 2000, he joined austriamicrosystems AG, where he currently works as an EMC R&D Engineer, focusing on the design optimization for electromagnetic compatibility of integrated circuits (EMC on chip-level). His research interests include the reduction of the electromagnetic emissions of integrated circuits using slew rate controlled output drivers or on-chip decoupling as well as improving the measuring methods to characterize the EMC of integrated circuits (IEC 61967 and IEC 62132). During his research activities, he has written several papers and technical articles in the field of electromagnetic compatibility of integrated circuits.

Dr. Deutschmann is a member of the IEEE EMC Society and of the TC47a of the IEC.

References

[i] IEC 61967-1: "Integrated circuits - Measurement of electromagnetic emissions, 150 kHz to 1 GHz - Part 1: General conditions and definitions", 47A/632/FDIS

[ii] IEC 62132-1: "Integrated circuits - Measurement of electromagnetic immunity, 150 kHz to 1GHz - Part 1: General and definitions", 47A/618/CD

[iii] IEC 61967-3: "Integrated circuits - Measurement of electromagnetic emissions, 150 kHz to 1 GHz –Part 3: Measurement of radiated emissions, surface scan method (10 kHz to 3 GHz)", 47A/620/NP, New Work Item Proposal, Date of proposal: Jul. 2001

[iv] "Universal testboard for measurement of EMC of ICs", 47A/552/NP, New Work Item Proposal, Date of proposal: February 1999

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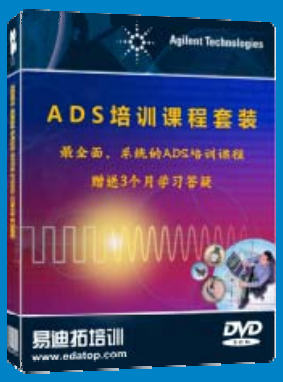

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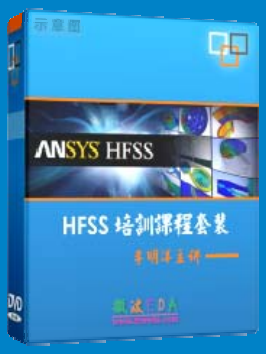

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