High-Speed Backplanes Pose New Challenges to Comms Designers

As backplane speeds move beyond 3 Gbit/s, designers will encounter problems not seen at lower rates. Fortunately, through the use of modeling techniques, designers can tackle these issues head on.

The operating data rates of current state-of-the-art backplane serial links are in the 2.5- to 3.125-Gbit/s range. As silicon becomes available that can support higher data rates into the 5- and 10-Gbit/s range, comm system designers are looking for ways to support these higher rates within their existing backplanes.

In the 5- to 10-Gbit/s range, the technical challenges created by phenomenon such as reflections and crosstalk increase. In addition, new voltage- and timing-related challenges have arisen that typically do not exist in lower data rate ranges. These include skin effect, dielectric loss, inter-symbol interference (ISI), and via stub effect.

To overcome these challenges, system designers must develop accurate and efficient models for both the active and the passive components of the system. Silicon vendors also need channel models to successfully design proper on-chip circuits for implementing various techniques like equalization and reflection cancellation. By modeling the known deterministic effects of the channel, signal-integrity related problems can be understood, and techniques can be developed to minimize their impacts.

To develop a backplane model, individual models for connectors, packages, PCB traces and vias are needed. In this article, we'll examine the technical challenges that must be overcome to support 5- to 10-Gbit/s rates, and the corresponding channel model requirements.

Channel Impairments

As the data transfer rate on the channel increases, "old" problems are exacerbated, and "new" problems arise that must be addressed. Figure 1 shows the key timing and voltage related impairments that must be addressed as data rates increase.

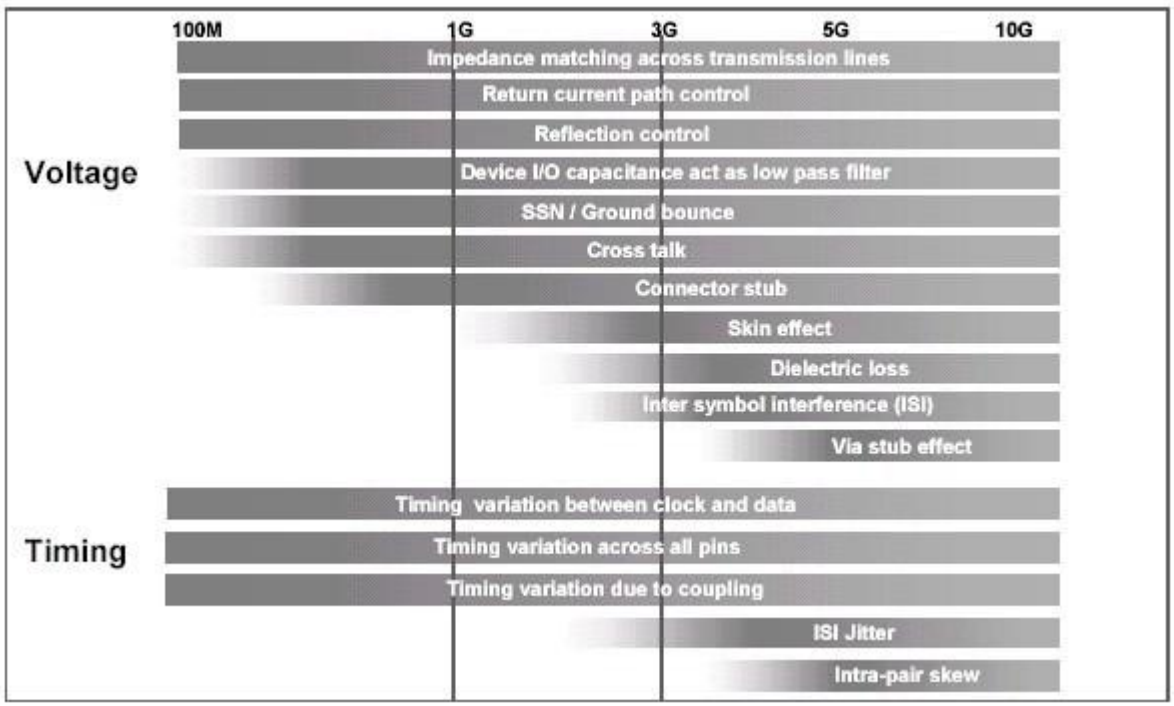

Figure 1: Above 3 Gbit/s, backplane transmission becomes a major challenge.

Figure 1 is divided into three regions of interest:

- **The 100 Mbit/s to 1 Gbit/s region**
- **The 1 to 3 Gbit/s region**
- **The 3 to 10 Gbit/s region**

The 100 -bit/s to 1-Git/s region is the better understood of the three. In this range the designer must compensate for the issues listed in the above drawing and remove fixed errors such as impedance mismatch and data/clock skew issues.

In the 1- to 3-Gbit/s range, the designer must make adjustments that are a function of the channel's electrical behavior, such as channel loss and distortion. These quantities are typically not known when the silicon is designed. Consequently, a feedback loop can be used to adjust the variables of concern. For example, the transmit driver output swing driving into a lossy channel can be adjusted by a feedback loop sensing the input swing at the far end receiver. The objective in this example is to overdrive the channel and compensate for its losses.

Above 3 Gbit/s, the existing variables become harder to manage, and new variables begin to emerge as shown in the above drawing. These include skin effect, dielectric loss, intersymbol interference (ISI), via stub effect, ISI jitter, and inter-pair skew. Let's look at these six in more detail starting with skin effect.

1. Skin Effect

Skin effect is a physical phenomenon related to high frequency transmission on a wire. At very high frequencies, the electromagnetic field of the wire causes most of the electrical current to become crowded at the edges of the wire. This phenomenon alters the distribution of the signal current throughout the wire and changes the effective resistance on the wire. The resulting effect is increased signal attenuation at higher frequencies.

2. Dielectric Loss

There are a number of PCB dielectric materials on the market today. The amount of dielectric loss in the material greatly affects signal integrity at high speeds. The lower the amount of dielectric loss, the less negative impact on the signal.

Figure 2 shows the total loss (conductor + dielectric) on a given trace at different speeds. The signal amplitude transfer function (output divided by input signal) is normalized at 1 where there is no attenuation in the channel.

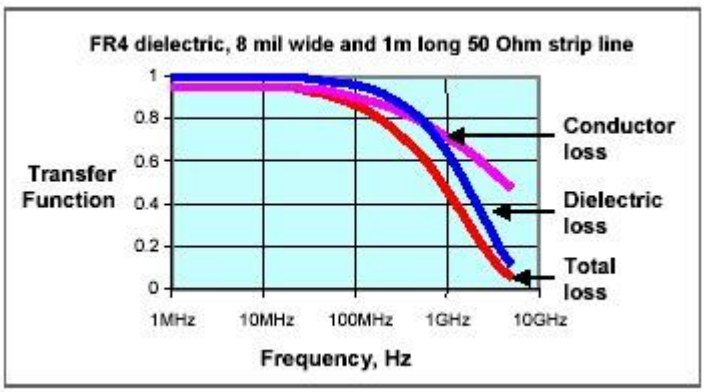

Figure 2: Loss as a function of frequency

Between 1 and 100 MHz, the amount of conductor and dielectric loss is negligible. Throughout this range, the signal transfer function remains at about 1. At 1 GHz the signal has decreased to approximately 0.5, half of its original strength. At speeds above 5 GHz the signal strength drops below 0.2, losing approximately 80% of its original strength. Thus, losses are a major issue at these high frequencies.

Although FR4 is the most commonly used material, it clearly does not have the best electrical characteristics when measured in terms of dielectric loss, as shown in the Figure 5. Still, FR4 is generally preferred due to its lower production costs.

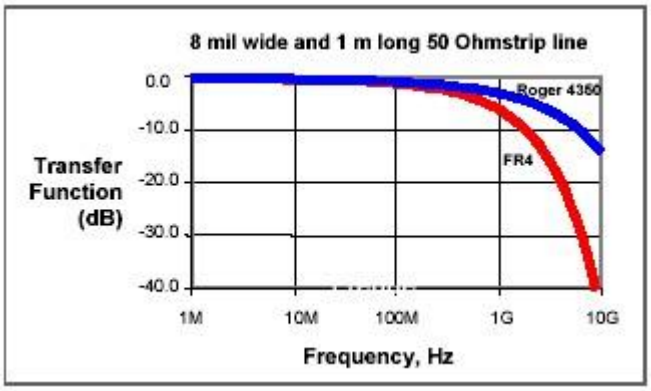

Figure 3: trace loss with FR-4 and Roger dielectrics

3. Intersymbol Interference

ISI is a phenomenon caused by the different propagation velocities of low and high frequencies throughout a channel. The end result is a spreading of bits, also known as pulse spreading. Stated differently, transmitting a square pulse through such a channel results in a widening and flattening of the pulse at the far end. This implies that each data bit of information overlaps with its adjacent bits. This overlap can cause major distortions of the signal. At high data rates and in long channels, the ISI can be so bad that it becomes impossible to recognize an eye pattern on the oscilloscope. This is a major phenomenon limiting data transmission, and must generally be addressed starting at the 2 to 3 Gbit data rates in most system backplanes.

4. Via Stub Effect

At high frequencies, via stubs can cause reflections in the signal. These stubs are common on all PCBs, but at lower speeds their effects are negligible. The thicker the backplane traces, the larger the via stubs, which in turn causes the amount of signal reflections to increase. Ideally, the stub length, and resulting stub delay, should be kept as short as possible.

5. ISI Jitter

ISI jitter is caused by intersymbol interference. Because the pulse's energy is seen to spread into the adjacent bits with ISI, this energy will combine with the previous and next bits respectively. The adding or subtracting of energy depends on the logical value of the current pulse, and the logical values of the previous and next bits. Since the amount of energy in each bit period varies as a result, the transition time between bits also varies. A movement in time of this transition time is called jitter. Therefore, bit-dependent jitter can result. This is known as ISI jitter.

6. Intra-pair skew

Intra-pair skew is the amount of skew between the two signals of a differential pair. This skew can be caused by variables such as a length mismatch between traces, non-uniform bends in the signal traces, via stubs, and via transitions.

Skew is normally measured as a percentage of the Unit Interval (UI). Even a slight amount of skew can dramatically impact the percentage of UI at high frequencies. For example, a 1% skew for a 30-inch trace correlates to a 5% UI mismatch at 1 Gbit/s and a 50% UI mismatch at 10 Gbit/s. This, in turn, reduces the data eye opening and increases the amount of jitter.

Equalization: Mitigating Impairments

Many of the channel impairments described above can be mitigated on-chip using equalization. This term is used to define circuits that can attenuate low frequencies and amplify high frequencies in either the transmit or receive directions, or both.

In one form of receive equalization, the incoming signal is sampled at different delay points. At each delay point, the signal is multiplied by a predetermined coefficient value. Each of the resulting values are then summed together to effectively recreate the signal as if it had just left the transmitter, effectively negating the effects of the various channel impairments described above.

Receive equalization is typically performed using a digital or analog adaptive filtering method. The equalization circuit examines the filtered signal output and adjusts the coefficients to optimize the signal quality through a feedback loop.

In contrast to the receive equalizer, the transmit equalizer boosts the high frequencies of a signal by a fixed amount before it is sent out. In theory, the negative effects of the previously mentioned variables will occur on the boosted portion of the signal, thereby allowing the overall signal quality at the receiver to more closely resemble that which was sent out by the transmitter. In other words, the transmitter pre-distorts the signal in the opposite way from that created in the channel so that a better quality signal can be seen at the receiver.

In both the transmit and receive path, there are two ways to set equalizer coefficients. The first is manual equalization. Also known as "set and forget", this coefficient setting technique is based on manual channel measurements. It can also be calculated on the basis of a single-bit-response (SBR) test through the channel.

The second method is to use an adaptive equalization approach. By using an adaptive algorithm such as Least Mean Square (LMS), the equalizer can optimize the signal quality by modifying the coefficients on a continuous basis. This allows the equalizer to adapt to changing conditions in the back-plane. A continuously adaptive method is far superior than the "set and forget" method because it adjusts to the changing environment automatically. This is relevant because environmental effects such as temperature and humidity changes can have a dramatic impact on the channel behavior.

System Modeling

Each of the points discussed above indicates an electrical variable that can impact

signal integrity over the backplane. To effectively manage the negative effects at each of these points, the physical structures impacting these electrical variables should be modeled. Once each physical structure is modeled (package, trace, via, etc.) an overall system model can be developed that is representative of the point-to-point trace from device to device.

Figure 4 shows a flow chart of the modeling process.

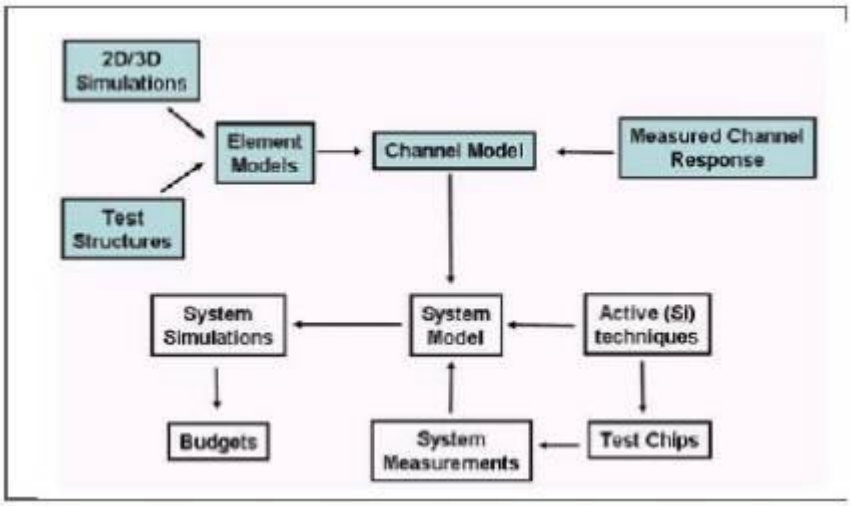

Figure 4: System model flow chart.

The flow chart shown in Figure 4 includes test structures, 2D/3D simulations, a channel model, a system model, test chips, and system simulations. Let's look at each block in more detail.

1. Test Structures

The test structures include measurements that have been made at the various points in the signal path. These include package-to-board via, line card trace, line card via, backplane connector, backplane via, and backplane trace.

Physical measurements are made on the electrical characteristics of each variable. Data from these measurements are then used to construct the overall channel model.

2. 2D and 3D Simulations

Another way to develop component models is via 2- or 3-dimensional simulation. In this case the simulator takes the size, length, thickness, and other relevant physical parameters and calculates the relative electrical characteristics for that component. These two types of models are then used to build the channel model shown in Figure 4.

3. Channel Model

The channel model includes everything except the silicon devices on each end. The channel model is built and tested and the results are compared against a measured channel response to determine whether the model is working correctly. Based on this correlation, the channel model is modified to match the results of the physical measurements. The goal is to have an accurate channel model at the frequencies of interest such that it can be used reliably as a predictor of behavior when simulating the entire system.

4. System model and Active Signal Integrity Techniques

The system model includes not only the channel model, but also the silicon devices at each end. At data rates below 1 Gbit/s, the system model and the channel model should indicate in most cases that the signal degradation can be addressed using standard fixed or feedback techniques, as discussed earlier. Above 1 Gbit/s, additional signal integrity (SI) techniques must be employed to maintain overall signal quality.

Active SI, or equalization, is required if the channel model simulation output dictates that additional steps must be taken to eliminate signal degradation. This is often the case above 1 Gbit/s, and generally always required in most systems above 3 Gbit/s.

4. Test chips and System Measurements

Once the active SI algorithm and circuit has been developed, test chips can be built to demonstrate that the equalization algorithms are working properly. System measurements can be taken on the test chip and on the overall system to ensure signal integrity from chip-to-chip. These results are then correlated to the system model to ensure the accuracy of the models.

5. System Simulations

With a well-correlated and stable system model, the overall system simulation can be done. The system simulation takes into account other variables such as:

- **Size of the channels in the chassis Number of potential cards**
- **Shortest distance over the backplane from card-to-card**
- **Longest distance over the backplane from card-to-card**

Using this information, the system simulator can interpolate the electrical characteristics for all other points in the chassis. For example, if the electrical characteristics between two points are measured, with the shortest distance being two inches and the longest distance being 10 inches, the system simulator can be used to calculate the electrical characteristics for all other points in between, provided a good system model has been built.

Wrap Up

The backplane is a complex system containing a number of variables that can impact signal integrity. The overall number of variables to be managed and the negative impact they have on signal quality increases with speed. At speeds over 3 Gbps, not only are the negative impact of existing variables increased, but new variables such as skin effect, dielectric loss, ISI, and via stub effect, must be taken into account.

The addition of physical components within a given point-to-point link also causes signal degradation. These include PCB traces, connectors, via stubs, and the actual silicon devices themselves. Each time another impairment is factored in, signal quality is reduced at high frequencies.

To overcome these challenges, system vendors must develop accurate and well-correlated models for both the active and the passive components of the system. Silicon vendors need quality channel models to successfully design proper on-chip circuits for implementing various techniques like equalization and reflection cancellation. By modeling all the known deterministic effects of the channel, signal-integrity related problems can be well understood and minimized.

About the Author

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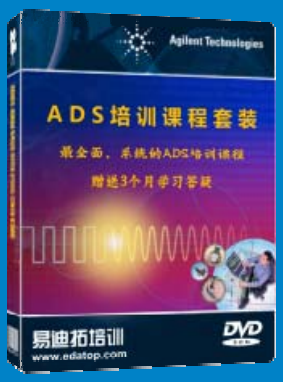

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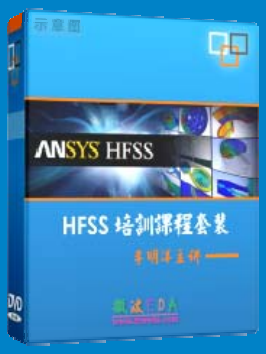

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