High-speed USB PCB Layout Recommendations

Introduction

High-speed USB operates at 480 Mbps with 400-mV signaling. For backwards compatibility, devices that are high-speed capable must also be able to communicate with existing full-speed USB products at 12 Mbps with 3.3V signaling. High-speed USB hubs are also required to talk to low-speed products at 1.5 Mbps. Designing printed circuit boards (PCBs) that meet these requirements can be challenging.

High-speed USB is defined in the Universal Serial Bus Specification Revision 2.0, located at http://www.usb.org. The organization that oversees the specification is the USB Implementers Forum. The USB-IF requires that all devices receive testing to show compliance to the specification and to ensure interoperability with other devices. Cypress recommends that designers pre-test their products for USB compliance before attending a USB Compliance Workshop.

This application note details guidelines for designing 4-layer, controlled-impedance, High-speed USB printed circuit boards to comply with the USB specification. This note is applicable to all Cypress High-speed USB solutions. Some Cypress High-speed USB chips have separate application notes that address chip-specific PCB design guidelines.

High-speed USB PCBs are typically 4-layer boards, though 6-layer boards may be helpful if the physical size is extremely tight and extra space is required for routing. The principles for both types of boards are the same. Cypress does not recommend using a 2-layer board for High-speed USB PCB design.

PCB design influences USB signal quality test results more than any other factor. This application note address five key areas of High-speed USB PCB design and layout:

- Controlled Differential Impedance
- USB Signals
- Power and Ground
- Crystal or Oscillator
- Troubleshooting

Controlled Differential Impedance

Controlled differential impedance of the D+ and D– traces is important in High-speed USB PCB design. The impedance of the D+ and D– traces affect signal eye pattern, end-of-packet (EOP) width, jitter, and crossover voltage measurements. It is important to understand the underlying theory of differential impedance in order to achieve a $90\Omega \pm 10\%$ impedance.

Theory

Microstrips are the copper traces on the outer layers of a PCB. A microstrip has an impedance, Z_0, that is determined by its width (W), height (T), distance to the nearest copper plane (H), and the relative permittivity (ε_r) of the material (commonly FR-4) between the microstrip and the nearest plane.

When two microstrips run parallel to each other cross-coupling occurs. The space between the microstrips (S) as related to their height above a plane (H) affects the amount of cross-coupling that occurs. The amount of cross-coupling increases as the space between the microstrips is reduced. As cross-coupling increases the microstrips' impedances decrease. Differential impedance, Z_{diff}, is measured by measuring the impedance of both microstrips and summing them.
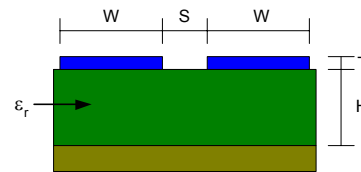

Figure 1. Microstrip Model of Differential Impedance

Figure 1 shows a cross-sectional representation of a PCB showing (from top to bottom) the differential traces, the substrate, and the GND plane. *Figure 2* provides the formulas necessary for estimating differential impedance using a 2D parallel microstrip model. *Table 1* provides the definition of the variables. These formulas are valid for $0.1 < W/H < 2.0$ and $0.2 < S/H < 3.0$. Commercial utilities can obtain more accurate results using empirical or 3D modeling algorithms.

$$Z_{diff} = 2Z_0\left(1 - 0.48e^{-0.96\frac{S}{H}}\right)$$

$$Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}}\ln\frac{5.98H}{0.8W + T}$$

Figure 2. Differential Impedance Formula

Table 1. Definition of Differential Impedance Variables

Variable	Description
Z_{diff}	Differential impedance of two parallel microstrips over a plane
Z_0	Impedance of one microstrip over a plane
W	Width of the traces
H	Distance from the GND plane to the traces
T	Trace thickness (1/2 oz copper $\cong$ 0.65 mils)
S	Space between differential traces (air gap)
ε_r	Relative permittivity of substrate (FR-4 $\cong$ 4.5)

Typical 62-mil, 4-layer PCB Example

The recommended stackup for a standard 62-mil (1.6-mm) thick PCB is shown in *Figure 3*. When this stackup is used with two parallel traces each with a width, *W*, of 16 mils and a spacing, *S*, of 7 mils the calculated differential impedance, Z_{diff}, is 87Ω.

With the same stackup it is possible to achieve a 90Ω ± 10% differential impedance on D+ and D– using other combinations of variables.

NOTE: .016 TRACES ARE 90-OHM DIFFERENTIAL IMPEDANCE
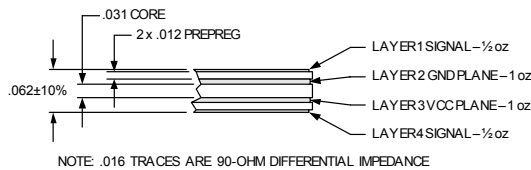
Figure 3. Typical Stackup for a 62-mil, 4-layer PCB

Recommendations

Use the following recommendations to achieve the proper differential impedance:

1. Consult with the PCB manufacturer to obtain the necessary design parameters and stackup to obtain a 90Ω ± 10% differential impedance on D+ and D–.

2. Set the correct trace widths and trace spacing for the D+ and D– traces in the layout tool.

3. Draw the proper stackup on the PCB Fabrication Drawing and require the PCB manufacturer to follow the drawing. See *Figure 3*.

4. Annotate the PCB Fabrication Drawing to indicate which trace widths are differential impedance. Also indicate what impedance and tolerance is required.

5. Request differential impedance test results from the PCB manufacturer.

USB Signals

There are five USB signals: VBUS, D+, D–, GND, and SHIELD. Their functions are shown in *Table 2*.

Table 2. USB Signals

Signal	Description
VBUS	Device power, +5 V, 500 mA (max)
D+ and D–	Data signals, mostly differential
GND	Ground return for VBUS
SHIELD	Cable shielding and receptacle housing

D+ and D–

Properly routing D+ and D– leads to high-quality signal eye pattern, EOP width, jitter, crossover voltage, and receiver sensitivity test results. The following recommendations improve signal quality:

1. Place the Cypress High-speed USB chip on the signal layer adjacent to the GND plane.

2. Route D+ and D– on the signal layer adjacent to the GND plane.

3. Route D+ and D– before other signals.

4. Keep the GND plane solid under D+ and D–. Splitting the GND plane underneath these signals introduces impedance mismatch and increases electrical emissions.

5. Avoid routing D+ and D– through vias; vias introduce impedance mismatch. Where vias are necessary (e.g., using mini-B connector) keep them small (25-mil pad, 10-mil hole) and keep the D+ and D– traces on the same layers.

6. Keep the length of D+ and D– less than 3 inches (75 mm). A 1-inch length (25–30 mm) or less is preferred.

7. Match the lengths of D+ and D– to be within 50 mils (1.25 mm) of each other to avoid skewing the signals and affecting the crossover voltage.

8. Keep the D+ and D– trace spacing, *S*, constant along their route. Varying trace separation creates impedance mismatch.

9. Keep a 250-mil (6.5-mm) distance between D+ and D– and other non-static traces wherever possible.

10. Use two 45° bends or round corners instead of 90° bends.

11. Keep five trace widths minimum between D+ and D– and adjacent copper pour. Copper pour when placed too close to these signals affects their impedance.

12. If the Cypress High-speed USB chip requires series termination and pull-up resistors on D+ and D– place their pads on the traces. Avoid stubs. Locate these resistors as close as possible to the chip. See *Figure 5* for reference.

13. Avoid common-mode chokes on D+ and D– unless required to reduce EMI. Common mode chokes typically provide little benefit for high-speed signals and can adversely affect full-speed signal waveforms.

VBUS, GND, and SHIELD

These recommendations for the VBUS, GND, and SHIELD signals improve inrush current measurements and reduce susceptibility to EMI, RFI, and ESD.

1. Route VBUS on the signal layer adjacent to the V_{CC} plane. This prevents it from interfering with the D+ and D– signals.

2. Filter VBUS to make it less susceptible to ESD events. This is especially important if the Cypress High-speed USB chip uses VBUS to determine whether it is connected or disconnected from the bus. A simple RC filter works well. See *Figure 4* for details. The filter should be placed closer to the USB connector than the USB chip.

3. Use 10 μF or less of capacitance on VBUS to prevent violating the USB inrush current requirements.

4. Connect the SHIELD connection to GND through a resistor. This helps isolate it and reduces EMI and RFI emissions. Keep this resistor close to the USB connector. Some experimentation may be necessary to obtain the correct value.

5. Provide a plane for the USB shield on the signal layer adjacent to the V_{CC} plane that is no larger than the USB header.
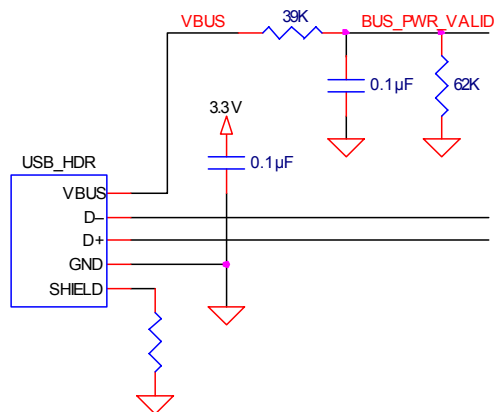
Figure 4. Schematic Showing the VBUS Filter, USB SHIELD-to-GND Resistor, and Decoupling Capacitor

USB Peninsula

If the location of a USB connector is near the edge of the PCB, consider placing it on a 'USB Peninsula' as described below. EMI and RFI are decreased by reducing noise on the V_{CC} and GND planes, as they are partially isolated from the rest of the board.

1. Make a cut in the V_{CC} and GND planes around the USB connector leaving a 200-mil (5-mm) opening for D+ and D– to preserve their differential impedance.
2. Use a 0.1-µF capacitor to decouple the V_{CC} and GND planes on the USB peninsula.
3. Place the SHIELD-to-GND resistor on the peninsula. If necessary, a second set of pads that connects SHIELD to the GND plane off the peninsula is useful.
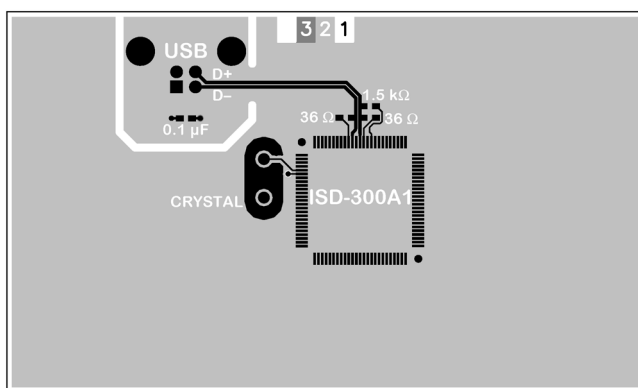

Figure 5. ISD-300A1 Layout Showing D+/D– Traces, Series Termination Resistors, USB Peninsula, and Crystal

4. Place a common-mode choke (if used, though not recommended) at the opening for D+ and D–.

Power and Ground

It is important to provide adequate power and ground for High-speed USB designs. The proper design is as important as layout technique.

V_{CC} and GND Planes

V_{CC} and GND planes are required for High-speed USB PCB design. They reduce jitter on USB signals and help minimize susceptibility to EMI and RFI.

1. Use dedicated planes for V_{CC} and GND.
2. Use cutouts on the V_{CC} plane if more than one voltage is required on the board (e.g., 2.5V, 3.3V, 5.0V).
3. Do not split the GND plane. Do not cut it except as described in 'USB Peninsula.' This reduces electrical noise and decreases jitter on the USB signals.

Power Traces

For situations where it is not necessary to dedicate a split plane to a voltage level (e.g., 5V or 12V), but the voltage is required on the board, route a trace instead. The following guidelines are recommended for power traces:

1. Keep the power traces away from high-speed data lines and active components.
2. Keep trace widths at least 40 mils to reduce inductance.
3. Keep power traces short. Keep routing minimal.
4. Use larger vias (at least 30-mil pad, 15-mil hole) on power traces.
5. Provide adequate capacitance (see below).
6. Use a chip filter if necessary to reduce noise.

Voltage Regulation

The following guidelines are recommended for voltage regulators to reduce electrical emissions and prevent regulation problems during USB suspend.

1. Select voltage regulators whose quiescent current is appropriate for the board's minimum current during USB suspend.
2. Select voltage regulators whose minimum load current is less than the board's load current during USB suspend. If the current draw on the regulator is less than the regulator's minimum load current then the output voltage may change.
3. Place voltage regulator(s) so they straddle split V_{CC} planes; this reduces emissions.

Decoupling and Bulk Capacitance

1. Provide 0.1-µF ceramic capacitors to decouple device power input pins. Place one cap per pin. Keep the distance from the pad to the power input pin less than 2.0 mm where possible.
2. Place bulk capacitors near the power input and output headers and the voltage regulator(s).
3. Provide 10–20 µF capacitance for the Cypress High-speed USB chip. Ceramic or tantalum capacitors are recommended. Electrolytic capacitors are not suitable for bulk capacitance.

4. Filter power inputs and outputs near the power headers to reduce electrical noise.

5. Follow chip-specific guidelines to properly isolate AV_{CC} from V_{CC} and AGND from GND.

6. Follow chip-specific guidelines to provide enough bulk and decoupling capacitance for AV_{CC}. Use ceramic or tantalum capacitors. Electrolytic capacitors are not suitable for bulk capacitance.

Crystal or Oscillator

A crystal or oscillator provides the reference clock for the Cypress High-speed USB chip. It is important to provide a clean signal to the USB chip and to not interfere with other high-speed signals, like D+ and D–.

1. Use a crystal or oscillator whose accuracy is 100 ppm or less.

2. Use a crystal whose first harmonic is either 24 or 30 MHz (depending on the Cypress High-speed USB chip). This requires less crystal start-up circuitry and is less error prone.

3. Place the crystal or oscillator near the clock input and output pins of the Cypress High-speed USB chip.

4. Keep the traces from the crystal or oscillator to the USB chip short.

5. Keep the crystal or oscillator traces away from D+ and D–.

6. Use ceramic capacitors that match the load capacitance of the crystal.

Troubleshooting

The USB electrical compliance tests often show mistakes in PCB layouts. The type of failure can point to the cause. *Table 3* shows some common problems and their possible causes for boards that fail high-speed or full-speed signal integrity or high-speed receiver sensitivity tests.

Conclusion

With the transition from 12 Mbps to 480 Mbps, printed circuit boards must be designed to meet USB electrical requirements. This is best achieved by using controlled impedance PCBs, properly laying out D+ and D–, and adequately decoupling the V_{CC} and GND planes to keep them electrically quiet.

Cypress Semiconductor provides a variety of High-speed USB development and reference design kits. These are helpful to see design examples and contain chip-specific design guidelines.

Table 3. Troubleshooting High-speed USB PCBs

Common Problem	Possible Causes
The high-speed or full-speed signal integrity tests show excessive jitter.	There is an impedance mismatch on D+ and D–.
	A noisy trace is located too close to D+ and D–.
	A common-mode choke is interfering.
	An active component (e.g., voltage regulator, SRAM, etc.) is not properly decoupled.
	AV_{CC} and AGND are not properly isolated or may not have enough bulk capacitance with a low ESR.
The EOP is not detected or out of spec during high-speed or full-speed signal integrity testing.	A common-mode choke is interfering with the EOP.
The crossover voltage is out of the specified range.	The trace lengths of D+ and D– are not matched.
	There is an impedance mismatch on D+ and D–.
The voltage level at the beginning of the high-speed chirp is too high when coming out of suspend.	The voltage regulator is unable to maintain 3.3V at 100 µA.
Receiver sensitivity is below the acceptable limit.	There is a split in the GND plane underneath D+ and D–.
	A common-mode choke is interfering.
	AV_{CC} and AGND are not properly isolated or may not have enough bulk capacitance with a low ESR.
Inrush current is above the acceptable limit.	Reduce bulk capacitance on VBUS. If designing a bus-powered solution employ a soft-start circuit so all of the capacitance isn't filled at once.

All product or company names mentioned in this document may be the trademarks of their respective holders.

射 频 和 天 线 设 计 培 训 课 程 推 荐

易迪拓培训(www.edatop.com)由数名来自于研发第一线的资深工程师发起成立，致力并专注于微波、射频、天线设计研发人才的培养；我们于 2006 年整合合并微波 EDA 网(www.mweda.com)，现已发展成为国内最大的微波射频和天线设计人才培养基地，成功推出多套微波射频以及天线设计经典培训课程和 ADS、HFSS 等专业软件使用培训课程，广受客户好评；并先后与人民邮电出版社、电子工业出版社合作出版了多本专业图书，帮助数万名工程师提升了专业技术能力。客户遍布中兴通讯、研通高频、埃威航电、国人通信等多家国内知名公司，以及台湾工业技术研究院、永业科技、全一电子等多家台湾地区企业。

易迪拓培训课程列表：http://www.edatop.com/peixun/rfe/129.html

射频工程师养成培训课程套装

该套装精选了射频专业基础培训课程、射频仿真设计培训课程和射频电路测量培训课程三个类别共 30 门视频培训课程和 3 本图书教材；旨在引领学员全面学习一个射频工程师需要熟悉、理解和掌握的专业知识和研发设计能力。通过套装的学习，能够让学员完全达到和胜任一个合格的射频工程师的要求…

课程网址：http://www.edatop.com/peixun/rfe/110.html

ADS 学习培训课程套装

该套装是迄今国内最全面、最权威的 ADS 培训教程，共包含 10 门 ADS 学习培训课程。课程是由具有多年 ADS 使用经验的微波射频与通信系统设计领域资深专家讲解，并多结合设计实例，由浅入深、详细而又全面地讲解了 ADS 在微波射频电路设计、通信系统设计和电磁仿真设计方面的内容。能让您在最短的时间内学会使用 ADS，迅速提升个人技术能力，把 ADS 真正应用到实际研发工作中去，成为 ADS 设计专家…

课程网址： http://www.edatop.com/peixun/ads/13.html

HFSS 学习培训课程套装

该套课程套装包含了本站全部 HFSS 培训课程，是迄今国内最全面、最专业的 HFSS 培训教程套装，可以帮助您从零开始，全面深入学习 HFSS 的各项功能和在多个方面的工程应用。购买套装，更可超值赠送 3 个月免费学习答疑，随时解答您学习过程中遇到的棘手问题，让您的 HFSS 学习更加轻松顺畅…

课程网址：http://www.edatop.com/peixun/hfss/11.html

CST 学习培训课程套装

该培训套装由易迪拓培训联合微波 EDA 网共同推出，是最全面、系统、专业的 CST 微波工作室培训课程套装，所有课程都由经验丰富的专家授课，视频教学，可以帮助您从零开始，全面系统地学习 CST 微波工作的各项功能及其在微波射频、天线设计等领域的设计应用。且购买该套装，还可超值赠送 3 个月免费学习答疑…

课程网址：http://www.edatop.com/peixun/cst/24.html

HFSS 天线设计培训课程套装

套装包含 6 门视频课程和 1 本图书，课程从基础讲起，内容由浅入深，理论介绍和实际操作讲解相结合，全面系统的讲解了 HFSS 天线设计的全过程。是国内最全面、最专业的 HFSS 天线设计课程，可以帮助您快速学习掌握如何使用 HFSS 设计天线，让天线设计不再难…

课程网址：http://www.edatop.com/peixun/hfss/122.html

13.56MHz NFC/RFID 线圈天线设计培训课程套装

套装包含 4 门视频培训课程，培训将 13.56MHz 线圈天线设计原理和仿真设计实践相结合，全面系统地讲解了 13.56MHz 线圈天线的工作原理、设计方法、设计考量以及使用 HFSS 和 CST 仿真分析线圈天线的具体操作，同时还介绍了 13.56MHz 线圈天线匹配电路的设计和调试。通过该套课程的学习，可以帮助您快速学习掌握 13.56MHz 线圈天线及其匹配电路的原理、设计和调试…

详情浏览：http://www.edatop.com/peixun/antenna/116.html

我们的课程优势：

※ 成立于 2004 年，10 多年丰富的行业经验，

※ 一直致力并专注于微波射频和天线设计工程师的培养，更了解该行业对人才的要求

※ 经验丰富的一线资深工程师讲授，结合实际工程案例，直观、实用、易学

联系我们：

※ 易迪拓培训官网：http://www.edatop.com

※ 微波 EDA 网：http://www.mweda.com

※ 官方淘宝店：http://shop36920890.taobao.com