PADS 9.0
Release Highlights

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PADS 9.0

PADS 9.0 introduces exciting new functionality to the PADS flow, including PADS Layout, PADS Router, PADS Logic, DxDesigner, and introduces new tools and functionality to improve productivity. Improvements with integration have been made throughout the flow. As with all releases, it also includes a significant number of defect fixes: see the Release Notes on the web.

The primary objectives for PADS 9.0 include:

- Enhanced Layout / Router integration
- SMS tool integration
- Differential pair and Accordion improvements
- Additional Pad shape definitions
- IPC-D-356 Net list output
- Flat DXF
- Keepout area for Accordions
- Single-sided board DRC
- Update from Library for Logic

Updated Licenses

If you received a 2009 license file prior to the release of PADS 9.0, you need to obtain a new license file that contains "**xxxx**" to enable new functionality. It is available at:

http://supportnet.mentor.com/myaccount/index.cfm?fa=user.authCodeForm

For help with installing the license file refer to TechNote MG59655

http://supportnet.mentor.com/reference/technotes/public/technote.cfm?tn=mg59655

The DxDesigner licensing is flow specific. Thus, a DxDesigner schematic created in Expedition cannot be modified in the PADS flow, and vice-versa.

For additional information on licensing, refer to the *Licensing Mentor Graphics Software* manual.

PADS Logic

Improvements to PADS Logic include enhancements to the library for updates and comparisons.

Compare and Update From Library

Designers want to ensure they use the latest library definition for symbols and components. PADS Logic can now compare parts and symbols in the design to those in the library. Any differences are reported, and the user can then choose to update the components in the design where differences are detected, to those in the library. A time stamp is now given to each part and symbol that will be compared, as well as attributes, labels, pins, gates, and much more.

PADS Layout

PADS Layout has been extensively enhanced and improved, with focus on better integration with other Mentor Graphics products.

PADS Layout /Router Integration

Switching between Layout and Router has been simplified, and a new button has been added to the toolbar in both PADS Layout and PADS Router, making moving data from one environment to the other much quicker and easier, enhancing designer productivity.

From PADS Layout to PADS Router

When the **Switch to Router** button is clicked, PADS Layout saves and closes the PADS layout database. Then, it launches and loads the data in PADS Router. PADS Layout remains open.

From PADS Router to PADS Layout

When the **Switch to Layout** button is clicked, PADS Router saves and closes the PADS Router database. Then, it launches and loads the data in PADS Layout. PADS Router remains open.

Differential Pair Improvements

Several improvements have been made to PADS 9.0 in the way differential pairs are handled. First, pad entry calculations have been updated to allow more symmetric traces for short runs

of differential pairs. The result is shorter, cleaner, and higher-yield differential pairs, providing better performance as well.

Second, diff pair tuning has been added. Accessed through the Tools>Options menu, these new parameters allow correction accordions when tuning. You can enable/disable the creation of the correction accordions in the gap portion, and restrict their use to situations where the length difference is greater than the matched length tolerance.

Accordion Keepouts

A new keepout type, accordion keepouts, has been added in PADS 9.0. These are recognized by PADS Router during auto routing and interactive routing.

When routing nets that have minimum length constraints, on occasion, PADS Router will route a trace outside a large pin device such as a BGA, then immediately add length with accordions. This can block channels, preventing other traces from entering/exiting the BGA. An accordion keepout can now be added around the device. The router will then be forced to continue routing out of the device, through the accordion keepout, before it can add the accordion pattern. The benefit is that there are fewer blocked channels, and better routability.

IPC- D- 356 Net List

IPC-D-356 and IPC-D-356A net list files can now be generated directly from PADS Layout. These files can be used to verify a net list against Gerber files.

Flat DXF Output

A new DXF file format can now be exported from PADS Layout. Flat DXF allows the user to select specific data to be exported to the .dxf file. The previous hierarchical file is still available.

Flat DXF files give results in smaller, more manageable files with only the selected data included. In addition, flat DXF files allow easier integration with mechanical tools.

Rounded and Chamfered Corners on Pad Stacks

Pad stacks can now be defined with rounded or chamfered corners. Corner types can now be defined at 90 degrees, Chamfered, or Rounded, and a radius can be set if Rounded or Chamfered is selected. In addition to customer requests for this function, it is also a requirement of RoHS.

Single-Sided Board DRC Verification

Single-sided boards with non-plated through holes are now recognized in Verify Design. If "Single-sided board support" is enabled, the connectivity checking algorithm will no longer report connectivity errors for component pins with non-plated drill holes. Decals with plated drills will be considered in CAM as non-plated drills.

3D Viewer

PADS 9.0 adds a three-dimensional viewer. If the Geometry.Height attribute has a value, the viewer is enabled. It can display vias and traces in 3D. The viewer provides controls for zoom, and rotate. An upgrade is available to additional functionality, including mechanical parts and enclosures for a more accurate view of the system design to observe any possible obstructions.

PADS Router

Accordions with Arcs

Accordions with arcs are a key requirement for high-speed designs.

To meet the high speed requirements, PADS 9.0 has added arc generation to PADS Router during interactive or automatic routing of accordions. The Tools> Options> Tune/Diff Pairs dialog has been updated with a "Use arcs in miters" check box. The Miter ratio setting controls the radius of the arc. Miter settings are applicable to accordions created in both auto and interactive modes. The Miter ratio controls both arcs and mitered corners for accordions.

Preserve Arcs During Smooth

Another item has been added in the Options> Routing dialog, "Preserve arcs during smooth", which maintains previously-created arcs during any "smooth" operation.

Miters Autorouting Pass

The Miters autorouting pass has been updated and can now create arc miters by using the Options> Routing>Miters setting.

High Speed Component Rules

A new setting in Options>General>Display Settings, “Distinguish component rules traces,” allows the user to easily identify traces which have component rules associated with them.

New Tuning Parameters

In Options> Tune/Diff Pairs, new tuning parameters, “Maximum amplitude” and “Maximum hierarchy level” have been added. In this same tab, a new setting has been added to control how much extra length is added to a net above that required by the matched length group tolerance by percentage. This setting is applicable for all matched length groups, including differential pairs and individual traces.

Automation

Additional automation objects and methods have been added to PADS Layout, Router, and Logic. Please refer to the online help for a complete description of these.

Manufacturing Support

PADS 9.0 adds support for a number of manufacturing products, including Mentor Graphics visECAD and CAMCAD. These tools are optional add-ons to the PADS 9.0 flow.

visECAD

Support has been added to PADS 9.0 for visECAD, a tool for collaboration with viewing and markup capabilities. Any markups made in visECAD can be imported back into PADS Layout.

CAMCAD Professional

CAMCAD integration allows “push-button” transfer of a design from PADS Layout to CAMCAD. CAMCAD Professional provides a link between the Design and Manufacturing environments. CAMCAD Professional can provide DFM and DFT analysis of PCB layout data. It can also be used to create assembly, test and inspection output files for various manufacturing equipment.

DxDesigner

A number of functions in DxDesigner have been added or enhanced with the PADS 9.0 release. These are summarized in the following sections.

Navigator: Single Click

Until now, a single click in the Navigator would open the sheet or the InterConnect Table (ICT) corresponding to the selected object in the editing window. Multiple selection in the Navigator would open as many sheets or ICTs as selected objects. The more objects selected, the longer it takes to open all the windows.

Some Navigator operations do not need the window(s) to be opened (e.g. Copy). Now a single click on an object selects it, but does not trigger cross-probing to the editors nor open a new window. A double click on the object opens the editing window.

Navigator: Drag sheet

To change the sheet order in the Navigator, users can select a sheet and use the Move Up or Move Down command on the Right Mouse Button menu. In PADS 9.0 this is enhanced to allow dragging a sheet to another location in the sort order.

Hierarchical Property Propagation

Users can now set a Property on a block and automatically propagate it to all the components underneath. The property value is not enforced and can be changed manually in the hierarchy later.

Selection by Overlap

A new “Selection by Overlap” mode has been added to the current mode. This functionality can be enabled from the “Advanced” option section of the Settings dialog page.

Selection by Overlap selects an object when the object is clipped by the selection fence rather than by needing to be completely enclosed by the fence as in Select by Fence mode. To select using overlap, simply draw a fence area and clip the objects to be selected. Release the mouse button and the object is selected.

Ripped Net Spacing

While ripping bits of a bus, users can dynamically change the bit spacing by pressing the <Shift>+<Ctrl> keys and using the mouse wheel.

DxDataBook Configuration File

The DxDataBook configuration file can now be referenced as a project setting and the data stored in the project file (KEY DBCFile in the .prj file). The setting is available in the Project section of the Settings dialog.

This configuration file is now written out in ASCII (XML format), which enables scripting. The file can be opened in any web browser. Binary files are still supported and may be referenced in the project file.

Windowing Management

Managing the many windows available in DxDesigner is sometimes a difficult task, especially in a single monitor environment. Docking and Un-docking provides users with a way to conveniently lay out windows. However, by docking windows all around the main window, editing space is significantly reduced.

One way to preserve maximum editing space is to group the ancillary windows together. In PADS 9.0 the user can now drag a window and drop it into another window by placing the cursor on a square target. It will automatically create tabs to switch between the two windows. This mechanism is not limited to two windows, and tabs available at the bottom of the “grouped” window can be easily re-ordered.

Additional Checks in Verify

Over 30 new checks were added to Verify to prevent hardware failure risks. It includes more connectivity checks, Power and Ground checks, Device Specific checks, and others. Checks have been re-numbered and re-categorized.

Note that numbers, categories, and even descriptions can be changed by the user in the VerifyDefaults.ini file (.xml file). The categories defined in this file appear in the Verify toolbar so that users can view each group of checks separately.

An “All checks” option was also added to the menu.

Descriptions that appear at the bottom of the Verify dialog page in the Rules tab have been updated to provide more information about the checks.

Copy/Paste in ICT Viewer

Users can now Copy and Paste a partial or a complete view of the ICT Viewer Net properties and Symbol Properties tabs into MS Excel. Users can either select the rows or the columns.

- If columns are selected, the content of columns will be copied for all the rows.
- If rows are selected, the content of all columns will be copied for selected rows only.

Quick Connection View Enhancement

The Quick Connection View (QCV) utility has been enhanced in three areas:

- Power and Ground (P&G) nets can now be displayed separately. This capability gives users a quick overview of how the design is powered and can be useful to detect power issues.

  There is a new option that lists the implicit and explicit Power and Ground separately. Explicit P&G are manually added in the design through P&G tap symbols, which carry the Global Signal Name common property. The value of this property determines the name of the P&G net.

  Implicit P&G are defined in the Supply and NC tab of the Part Editor. This information does not appear explicitly in the editors and must be extracted from the Part Database.
- The Flat Net option shows which hierarchical nets belong to which flat net. Flat nets appear in the layout tool. A Compress Mode option removes any hierarchical reference and lists the connections to actual components on one line.
- A third option allows listing eventual properties and/or Net Class set to the nets. Net Classes only apply to flat nets, so Flat Net option must be ‘on’ to see them.

Copy/Replace sheet

The ability to Copy and Paste one or several sheets has been available for several releases. A “pasted” sheet is added at the end of the list with its number automatically incremented. Sheets can be moved up and down in the Navigator to change the order, which will be used by other utilities like DxPDF.

However, users would sometimes like to substitute one or more sheets of a block by the sheet(s) about to be pasted. The Paste algorithm has been modified to take into account selected sheet(s) in the destination block.

If one or more sheets are selected in the destination block, the paste command will delete it/them and replace it/them by the copied sheet(s). After deletion of the selected sheets, any name conflicts detected during paste are rectified by naming the pasted with _1 etc. to avoid conflict and loss of design data.

ICE: Import/Export ASCII File

One area where the tabular nature of the InterConnectivity Editor provides a true gain in productivity is Connector and Backplane connectivity entry.

The capability to import ASCII files describing the connectivity of standard connectors or backplanes is now available in PADS 9.0. The expected syntax of the ASCII file is shown below and consists of a few keywords to identify the parts followed by the PIN/NET connectivity.

It is also possible to export full or partial connectivity (depending on the selected objects) entered in ICE into an ASCII file or into the Clipboard. Once copied in the Clipboard the user can paste the selected connectivity into a spreadsheet like MS Excel.

ICE: Quick Connection of Global Signals

Utilization of global nets has been significantly improved in the InterConnectivity Editor.

The creation of a global net using the Add Power or Add Ground commands has been simplified as a net will automatically be added and connected to the tap (power/ground symbol) with the proper name as defined by the tap symbol Global Signal Name property value.

Power and Ground icons  are now used in ICE to easily identify the supply taps.

Connection to power and ground has also been improved in the Advanced Connect dialog page. Global nets of the design as well as nets carrying the “Power Supply Net” property are directly accessible from the dialog page.

Filters have been extended to support Power and Ground pin types which are now available in the New Symbol Editor (NSE).

Design Diagnostics

Design diagnostics have been built into both DxDesigner and CES. Diagnostics run when the user exits a DxDesigner project or closes CES. These diagnostics ensure that any minor issues resulting from unexpected users' operations (e.g. the user kills the server from Task Manager on Windows) can be identified and easily fixed with no impact on the design.

The diagnostics are not automatically run by default; they can be enabled by setting the appropriate check box in each application. To enable the DxDesigner Diagnostics check the check box in the Setup>Settings..>DxDesigner Diagnostics menu item. DxDesigner will always execute the diagnostics when a design is upgraded to the next release.

If issues are found in either application they are written to the output window and the user will be prompted to fix them automatically.

HyperLynx 8.0

Integration with HyperLynx 8.0 brings the fastest accurate analysis tools available for both Signal Integrity (SI) and Power Integrity (PI). HyperLynx 8.0 is enhanced with wizards to save time and increase accuracy with both configuring and executing simulations. In addition, Signal Integrity tools have been enhanced and a complete Power Integrity analysis tool has been added. These are briefly summarized here, and in more detail in *What's New in HyperLynx 8.0*, available at www.mentor.com/pcb.

HyperLynx PI

HyperLynx PI is a significant new tool that provides the fastest time to accurate results. With fragmented power planes, several voltages per board, and very small noise margins, it is no longer possible using the old "rules of thumb" to get a board with acceptably clean power.

Because of the complexities of PI analysis, HyperLynx PI introduces an easy-to-use wizard environment from which to set up and run analysis suites. Analyses can be run both pre- and post-layout, which can cut time and cost. Among the capabilities of HyperLynx PI are Voltage Drop Analysis, Current Density Analysis, and Power Distribution Noise Analysis.

A Decoupling Wizard and Bypass Analysis make quick work of determining the number, size, and location of bypass and decoupling capacitors. The wizard cuts time to a minimum.

HyperLynx SI

Improvements to the Signal Integrity analysis tool include the new wizards, and new support of advanced memory devices, including DDR2 and DDR3. This memory support function has become so easy to use with the wizards that tests can be defined in just a few minutes.

The SI tool can also co-simulate with the PI tool for complete signal and power analysis. Other enhancements include the Touchstone Transformer, Transmission Line models and coupling, and improvement to the Fast Eye function.

Other Enhancements

Simulation Sweeps

The Central Sweep Manager allows easy global views and controls of the sweep parameters.

Per-net or Per-pin stimulus is now available, which is excellent for locating crosstalk. There are also many enhancements to integration, allowing more efficient use of both tools.

DxDesigner to LineSim allows extraction of nets from DxDesigner for use in LineSim. Extraction of nets for use in LineSim is the starting point for topology-template definition refinement.

HyperLynx Analog

The PADS 9.0 release focus has been to increase general usability of board-level simulation solutions, from source definition through to symbol mapping.

Add Source Dialog

The *Add Source* dialog has been enhanced to provide more flexibility to the user as well as increase the usability of the dialog.

It is now possible to edit the *Source* definition from the main spreadsheet GUI; simple drop-down lists allow the user to choose from a list of nets within the design or enter the DC voltage by typing in a cell.

The addition of the check box in the left hand column allows the user to select or deselect individual sources for a specific simulation run. The user can now specify a range of sources that exercise different aspects of the design operation and then simply enable appropriate ones at the appropriate time.

Pin Mapping

The ability to map the component pins in the model to the component pins on the symbol for Spice models was delivered with the PADS2007.3 release. In PADS 9.0 this has been extended to include VHDL models too. The user can now associate a VHDL model to a symbol and then map the model and symbol pins through the simple to use dialog. The symbol pins are listed on the left and then the user can select the model pins using a drop down list, this greatly speeds the process.

Monte Carlo Analysis

As part of its statistical analysis capability, HyperLynx Analog provides Monte Carlo analysis simulation through the *Setup>Simulation* dialog. The user can apply a distribution to the passive components in the design. In previous releases, this distribution information was appended to the *Value* property. With the PADS 9.0 release, this information is now stored in a new property, *Distribution*, providing a much cleaner approach to both the schematic and simulation process.

HyperLynx BoardSim and LineSim

Integration with HyperLynx BoardSim provides significant board analysis capabilities. Users can go directly from PADS Layout to HyperLynx BoardSim and simulate crucial signals, or all the signals on the board if desired. Solutions to signal integrity, crosstalk, or timing problems can be explored from within BoardSim, or nets can be extracted into HyperLynx LineSim for powerful exploratory analysis. LineSim can also be used early on in the design phase to analyze crucial signals to determine routing constraints. HyperLynx allows for proactive problem identification, saving costly board spins and crucial time to market.

HyperLynx Thermal

Integration with HyperLynx Thermal allows quick and easy analysis of the thermal characteristics of PCBs. Users can go directly from their PADS layout into HyperLynx Thermal and generate board and component thermal profiles almost immediately. HyperLynx Thermal identifies excess component and board temperatures, as well as thermal gradients, using intuitive color maps.

Users can easily target board "hot spots" and solve thermal issues by analyzing effects of adding more copper, altering component placement, adding heat sinks, placing screws or standoffs, and more. HyperLynx Thermal allows for creation of systems free from thermal problems early in the design phase, and systems that will exhibit long-term reliable performance.