

Digital and analogue circuit design

Section 6

Outline



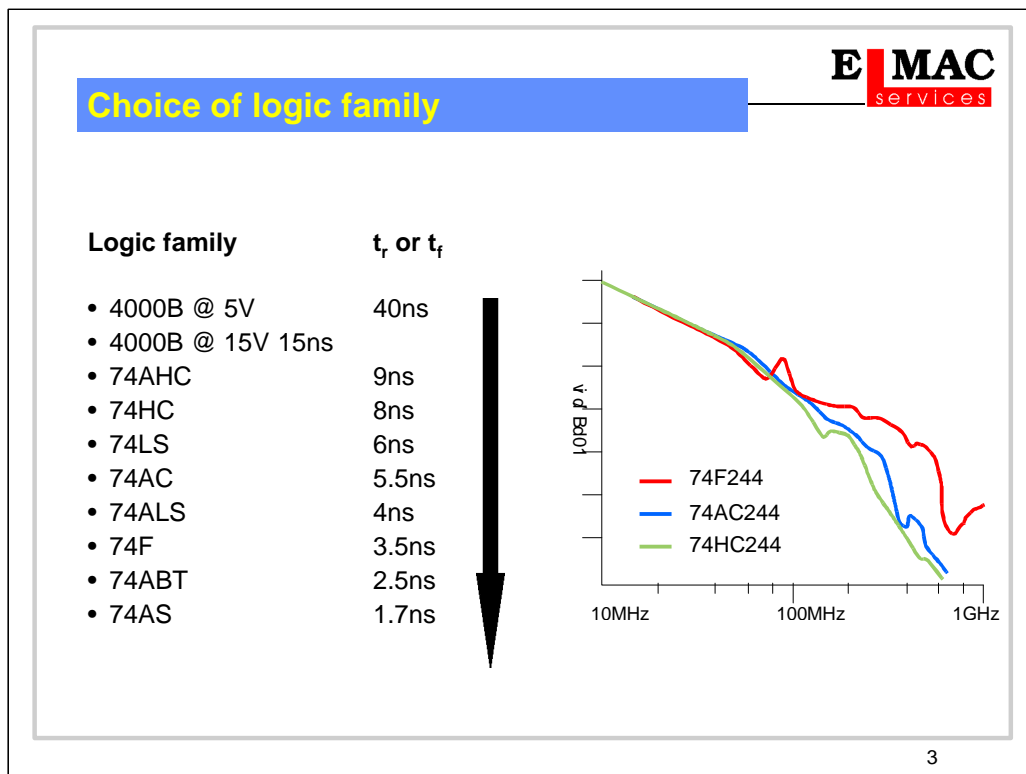
- emissions from logic circuits
- emissions from analogue circuits
- logic circuit immunity
- analogue circuit immunity

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Digital circuits are prolific generators of electromagnetic interference. High-frequency square-waves, rich in harmonics, are distributed throughout the system. The harmonic frequency components reach into the part of the spectrum where cable resonance effects are important. Analogue circuits are in general much quieter because high frequency squarewaves are not normally a feature. Nevertheless any analogue design which includes a high frequency oscillator must follow HF design principles, especially in regard to ground layout.

Some amplifier circuits are prone to oscillation in the MHz range, especially when driving a capacitive load, and these can cause unexpected emissions. The switching power supply is a serious cause of interference in the low frequency range since it is essentially a high-power squarewave oscillator.

Because the microprocessor is a state machine, processor-based circuits are prone to transient corruption. Great care is necessary to prevent any clocked circuit from being susceptible to incoming interference. The immunity of analogue circuits is improved by minimizing amplifier bandwidth, maximizing the signal level, using balanced configurations and electrically isolating or filtering I/O that will be connected to “dirty” external circuits.



The damage as far as emissions are concerned is done by logic edges which exhibit a fast rise/fall time (note that this is not the same as transition time and is rarely specified in data sheets; where it is, it is usually a maximum figure). Use the slowest logic family that will do the job; don't use fast logic for no reason. Where parts of the circuit must operate at high speed, use fast logic only for those parts and keep the clocks local.

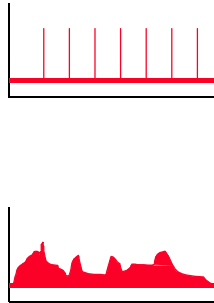
The graph shows the measured harmonics of a 10MHz square wave for three devices of different logic families in the same circuit. Note the emphasis in the harmonics above 200MHz for the 74AC and 74F types.

Radiation of emissions from a circuit containing logic devices is caused by the di/dt (changing current) flowing either in the pcb traces or in connected cables. The efficiency of these routes is proportional to F or F^2 and so emphasizes the higher frequency content; also, to reduce the rise time for a given circuit capacitance, the gate output current drive di/dt must be increased.

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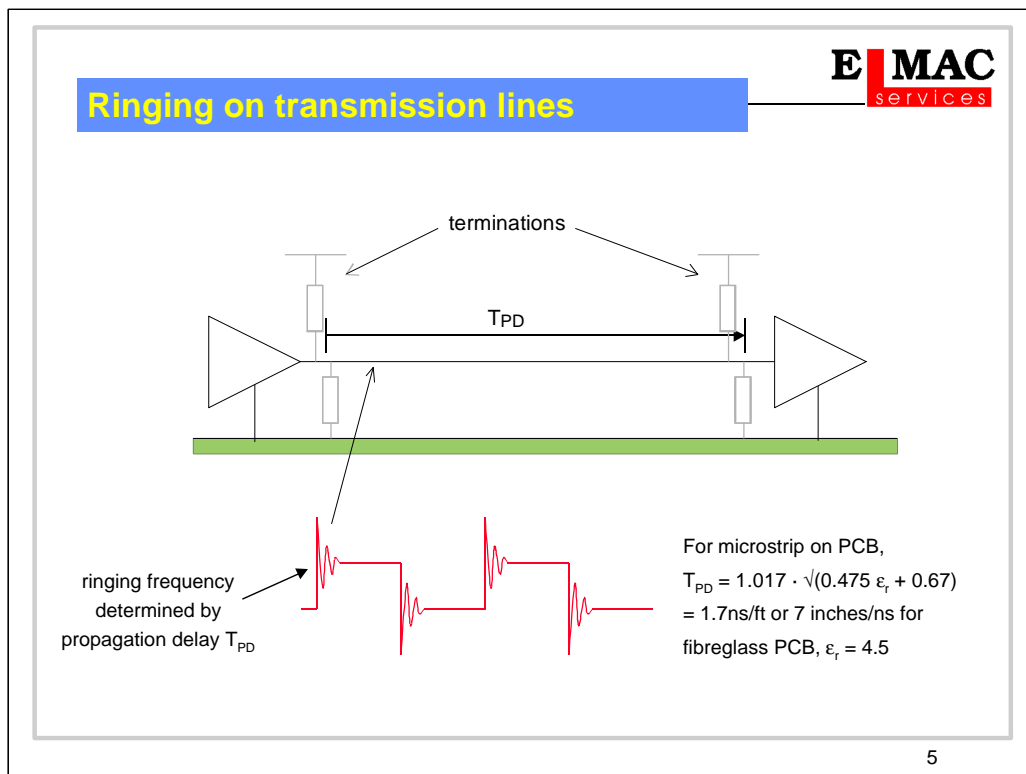
Clock and broadband emissions

- Pay most attention to:
 - clocks on backplanes and PCBs
 - data buses on backplanes and PCBs
 - video and other wideband signals



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The main source of radiation in digital circuits is the processor clock (or other system clocks) and its harmonics. All the energy in these signals is concentrated at a few specific frequencies. Since the radiated emissions standards do not distinguish between narrowband and broadband, these narrowband emissions should be minimized first, by proper layout and grounding of clock lines. Then pay attention to other broadband sources, especially data/address buses and backplanes, and video or high-speed data links. The least significant data/address bit usually has the highest frequency component of a bus and should be run closest to its ground return. Because backplanes carry all buses and clocks in the system, and carry a heavy capacitive loading, they should always use a multilayer board with a ground plane, and daughter board connectors should have a ground pin next to every clock or data pin.

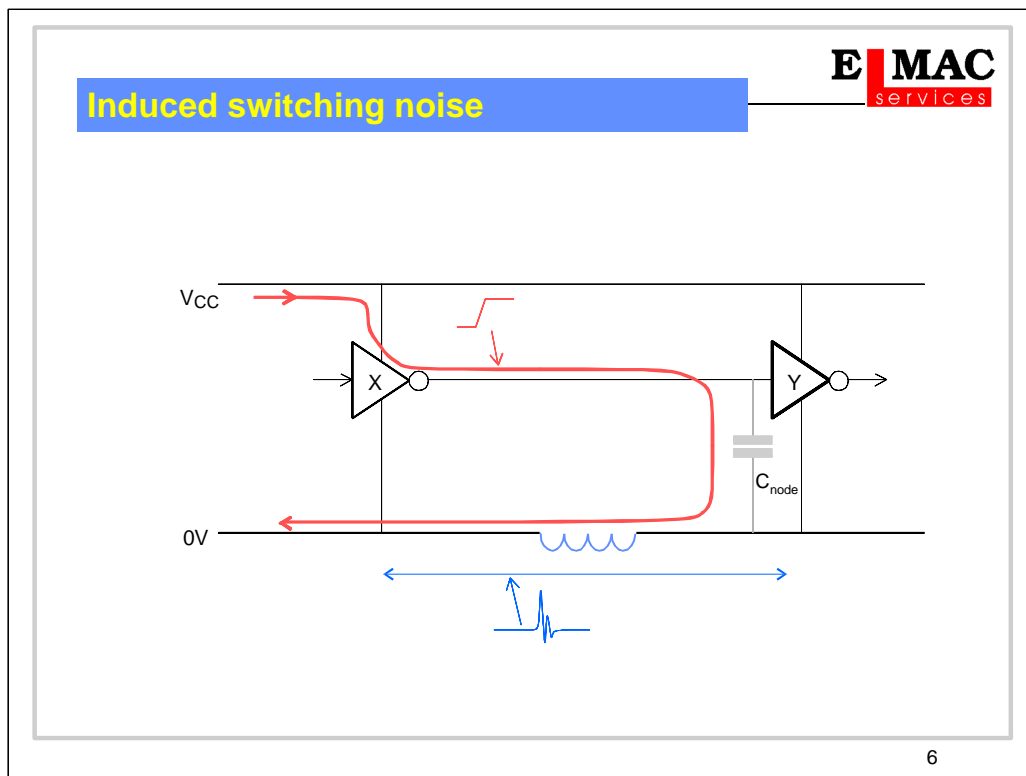


If data or clocks are sent down long lines, these must be terminated to prevent ringing. Ringing is generated on the transitions of digital signals when a portion of the signal is reflected back down the line due to a mismatch between the line impedance and the terminating impedance. A similar mismatch at the driving end will re-reflect a further portion towards the receiver, and so on. Severe ringing will affect the data transfer since it can exceed the device's input noise margin.

Aside from its effect on noise margins, ringing may also be a source of interference in its own right. The amplitude of the ringing depends on the degree of mismatch at either end of the line while the frequency depends on the electrical length of the line. A digital driver/receiver circuit should be treated as a transmission line, and therefore properly terminated, if

$$2 \times t_{PD} \times \text{line length} > \text{rise time}$$

where t_{PD} is the line propagation delay in ns per unit length

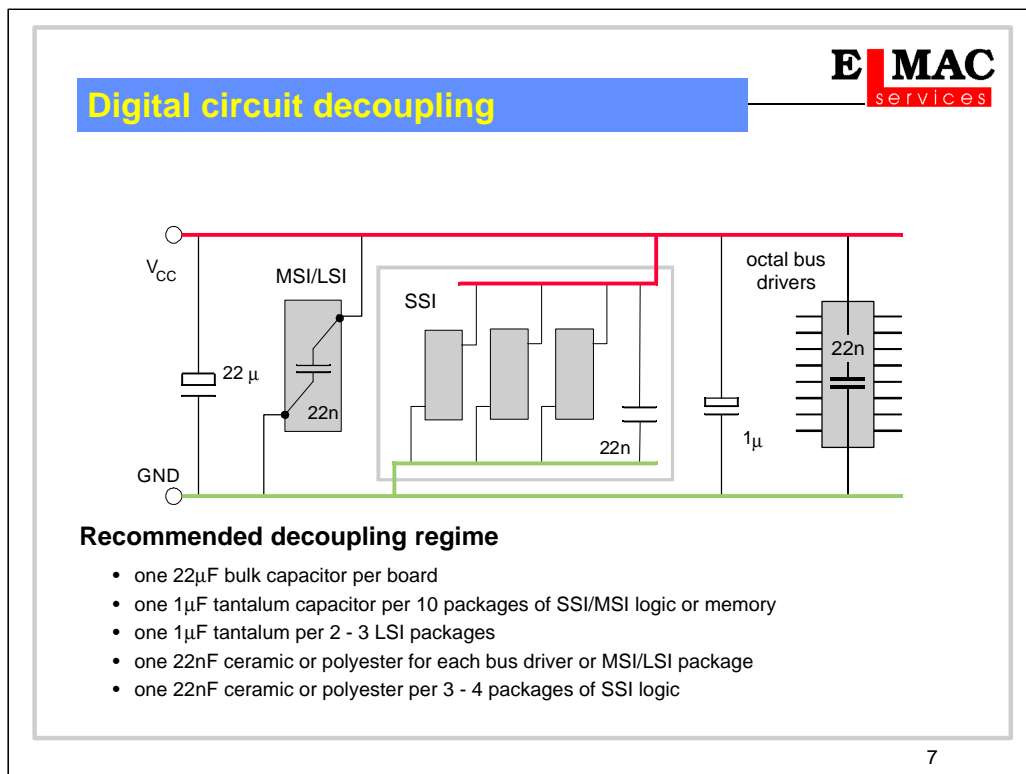


Noise is induced on the supply rails by the switching action of each logic gate in the circuit. As each gate changes state, a current pulse is taken from the supply pins because of the different device currents required in each state, the external loading, the transient caused by charging or discharging the node capacitance, and the conduction overlap in the totem-pole output stage. The supply current spike causes a disturbance in the supply voltage and also in the ground line, because of the inductive reactance of the lines. The equation which describes the voltage developed across an inductor is

$$V = -L \cdot di/dt$$

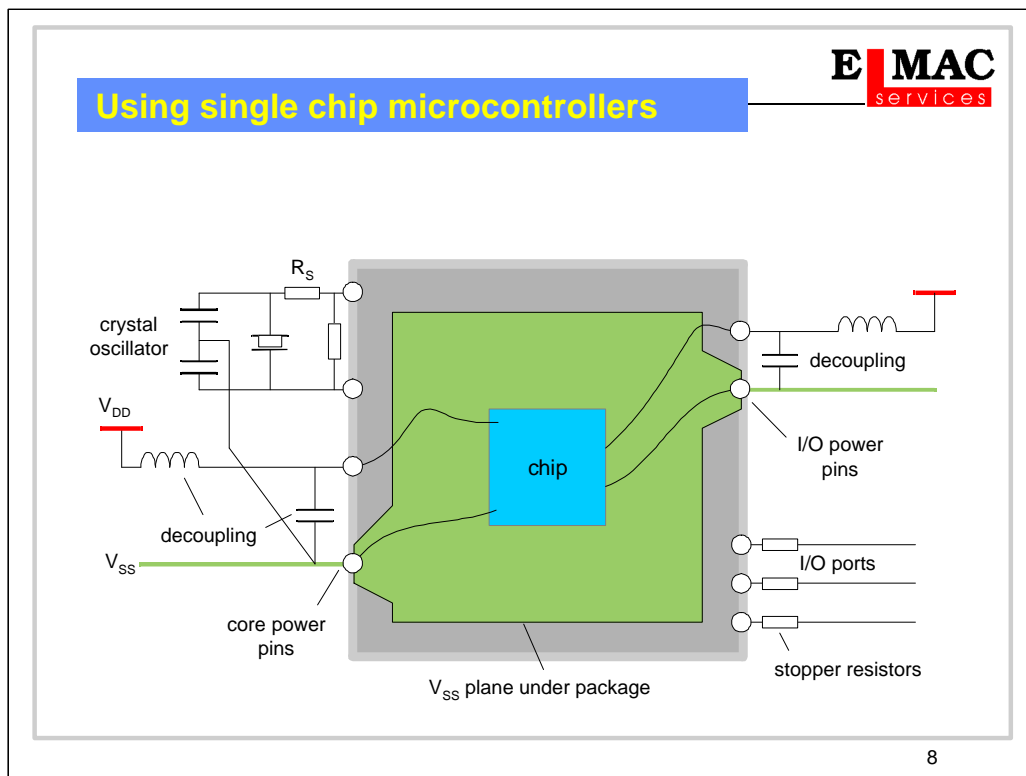
Pulses on a high-impedance ground line can easily exceed the noise threshold and cause spurious switching of innocent gates, as well as being responsible for emissions coupled out of the circuit.

The supply pin pulse current is magnified in synchronous systems when several gates switch simultaneously. A typical example is an octal bus buffer or latch whose data changes from $\#FF_H$ to $\#00_H$. If all outputs are heavily loaded a formidable current pulse - exceeding an amp in fast systems - will pass through the ground pin. Ground noise on a microprocessor board can be observed by hooking a wide-bandwidth oscilloscope to the ground line.



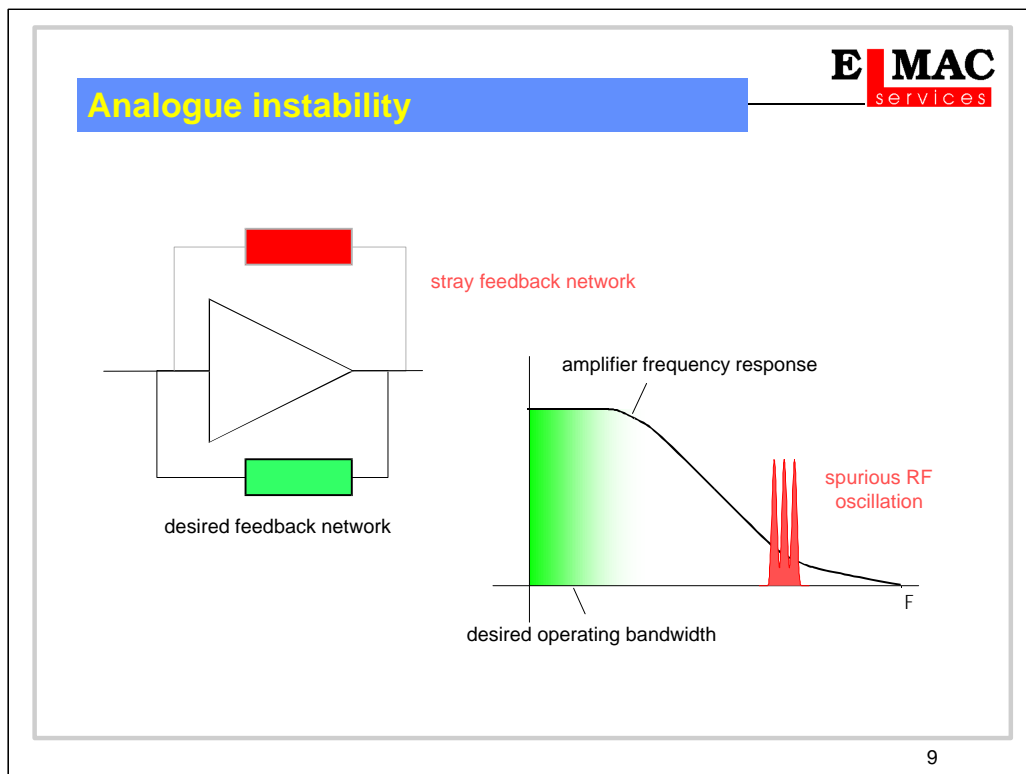
No matter how good the V_{CC} and ground connections are, track distance will introduce an impedance which will create switching noise from the transient switching currents. The purpose of a decoupling capacitor is to maintain a low dynamic impedance from the individual IC supply voltage to ground. This minimises the local supply voltage droop when a fast current pulse is taken from it. The capacitor must be located close to the circuit it is decoupling. "Close" in this context means less than half an inch for fast logic such as AS/ ALS-TTL or ECL, especially when high current devices such as bus drivers are involved, extending to several inches for low-current, slow devices such as 4000B-series CMOS.

The crucial factor when selecting capacitor type for high-speed logic decoupling is lead and package inductance rather than absolute value. Minimum inductance offers a low impedance to fast pulses. Small disk or multilayer ceramics, or polyester film types, are preferred; chip capacitors are even better.



RF emissions from digital circuits are minimized if all the high-speed signals are kept on chip, as is the case with single chip microcontrollers. For these devices the major contributors to emissions are the power supply connections, the crystal oscillator connections and any external bus to RAM or ROM.

Crystal oscillator components should be kept absolutely local to their pins, with no other tracks run past them and with a local ground return to the proper V_{SS} pin. Drive should be kept as low as possible with an appropriate series resistor R_s . Modern microcontrollers have two sets of V_{DD}/V_{SS} connections dedicated to the core and the I/O. These should be separately decoupled with capacitors adjacent to each pair of pins, and preferably isolated from the V_{DD} rail by low value series chokes, to keep transition currents circulating locally and not propagating into the rest of the supply. The optimum V_{SS} layout is a ground plane underneath the IC package connecting the two pins. Output pins may offer routes out of the device for residual ground noise, which can be attenuated by stopper resistors close to the package.

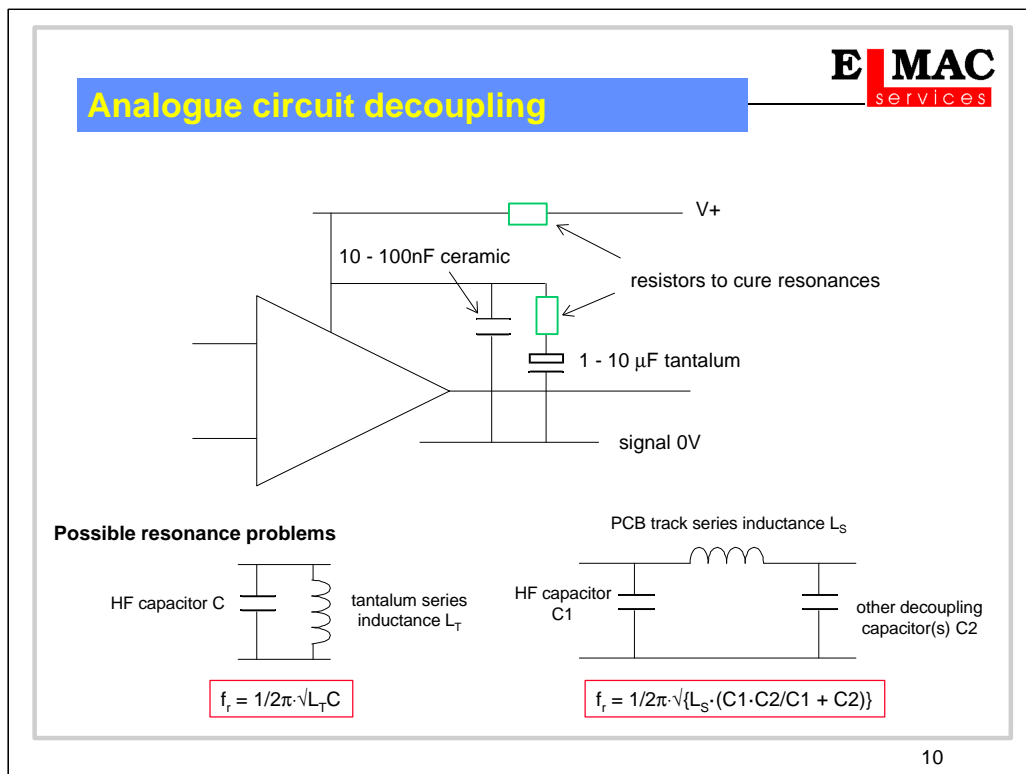


Analogue amplifier circuits may oscillate in the MHz region and thereby cause interference for a number of reasons:

- feedback-loop instability
- poor decoupling
- output stage instability


Capacitive coupling due to poor layout and common-impedance coupling are also sources of oscillation. Any prototype amplifier circuit should be checked for HF instability, whatever its nominal bandwidth, in its final configuration.

Feedback instability is due to too much feedback near the unity-gain frequency, where the amplifier's phase margin is approaching a critical value. It may be linked with incorrect compensation of an uncompensated op-amp.

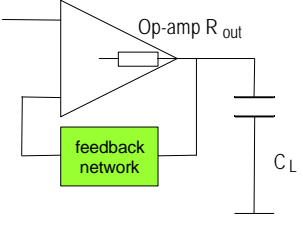


Power supply rejection ratio falls with frequency, and power supply coupling to the input at high frequencies can be significant in wideband circuits. This is cured by decoupling, but typical 0.01 - 0.1µF decoupling capacitors may resonate with the parasitic inductance of long power leads in the MHz region, so decoupling-related instability problems usually show up in the 1 - 10MHz range. Paralleling a low-value capacitor with a 1 - 10µF tantalum capacitor will drop the resonant frequency and stray circuit Q to a manageable level.

Note that the tantalum's series inductance could resonate with the ceramic capacitor and actually worsen the situation. To cure this, a few ohms resistance in series with the tantalum is necessary, though often the tantalum is lossy enough at HF not to need this. The input stages of multi-stage high gain amplifiers may need additional resistance in series with each stage's supply to improve decoupling from the power rails.

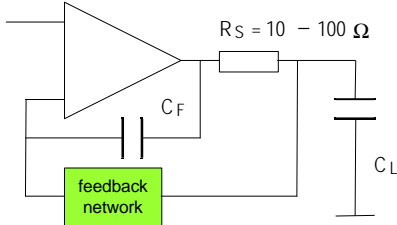


Output stage instability



Phase lag @ frequency $f = \tan^{-1}(f/f_c)$ degrees
 where $f_c = 1/2\pi \cdot R_{OUT} \cdot C_L$

Problem



Isolate a large value of C_L with R_S
 and C_F , typically 20pF

Solution

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Capacitive loads cause a phase lag in the output voltage by acting in combination with the op-amp's open-loop output resistance. This increased phase shift reduces the phase margin of a feedback circuit. A typical capacitive load, often invisible to the designer because it is not treated as a component, is a length of coaxial cable. Coax is capacitive until its length approaches a quarter-wavelength (i.e. as the frequency rises): for instance, 10 metres of the popular RG58C/U 50Ω type will be about 1000pF, but it will be a quarter wavelength at 4.95MHz allowing for velocity factor. The capacitance can be decoupled from the output with a low-value series resistor, and high-frequency feedback provided by a small direct feedback capacitor C_F which compensates for the phase lag caused by C_L .

If high output current is necessary a ferrite bead can be an acceptable substitute for R_S .

Digital immunity design



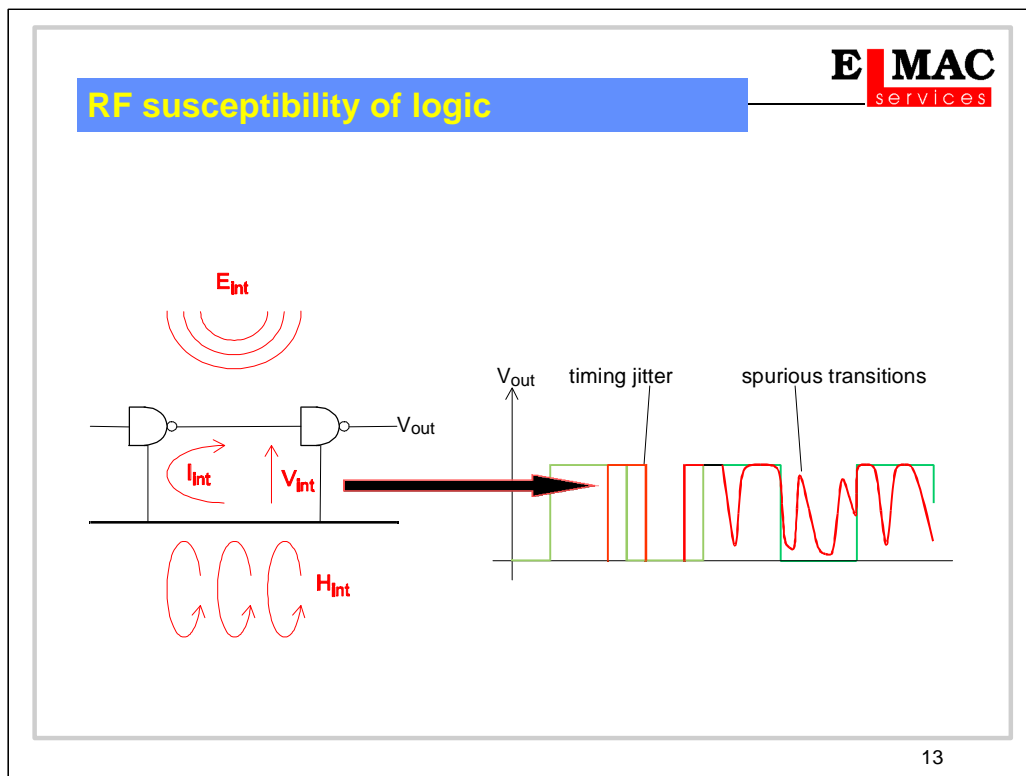
- Keep interference paths away from critical logic circuitry
 - layout
 - I/O filters and isolation
- Choose logic family for immunity, keep timing requirements relaxed
- Use a watchdog
- Adopt defensive programming tactics

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Most of the critical interference propagates via the grounding structure, whether it is common-mode RF or transients. Therefore, lay out the circuit to keep ground interference currents away from the logic circuits. If layout is not enough, filter the I/O leads or isolate them, to define a preferential safe current path for interference. Radiated RF fields that generate differential-mode voltages internally are dealt with in the same way as differential RF emissions, by minimizing circuit loop area.

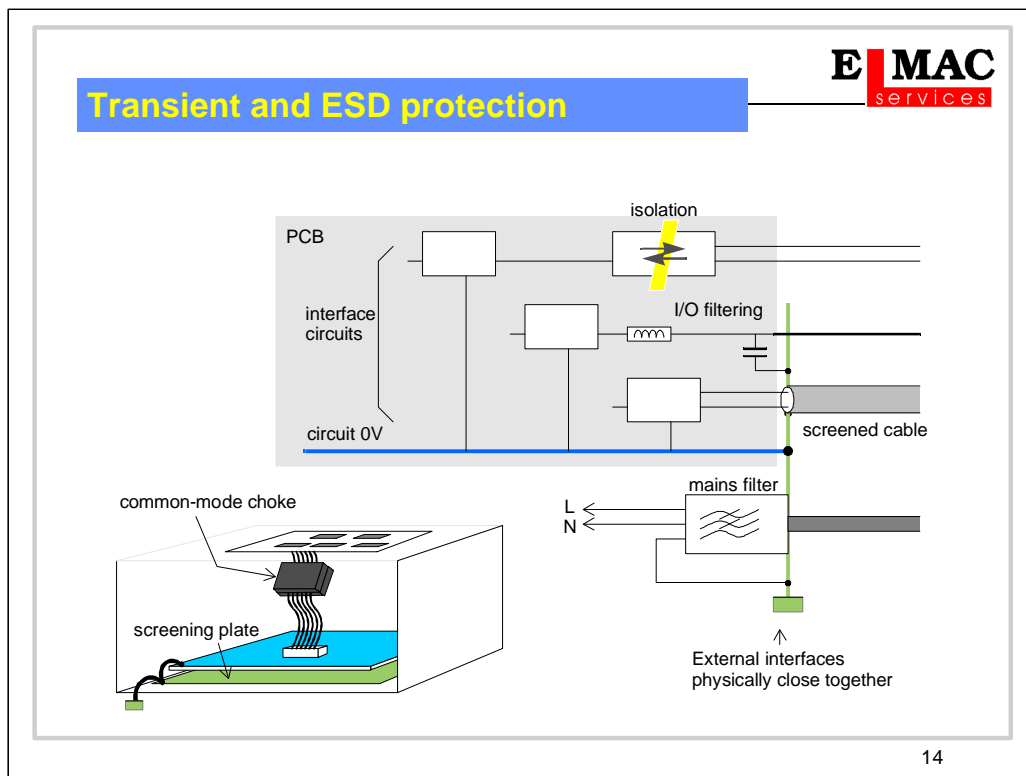
The best logic family for immunity will be one which has a high noise threshold and a low bandwidth – the faster its operation, the more susceptible to short pulses and RF it will be. Use synchronous design, and try to avoid edge-triggered data inputs wherever possible.

However good the circuit's immunity, there will always be a transient that will defeat it. Every microprocessor should include a watchdog, and software techniques should be employed that minimize the effects of corruption.



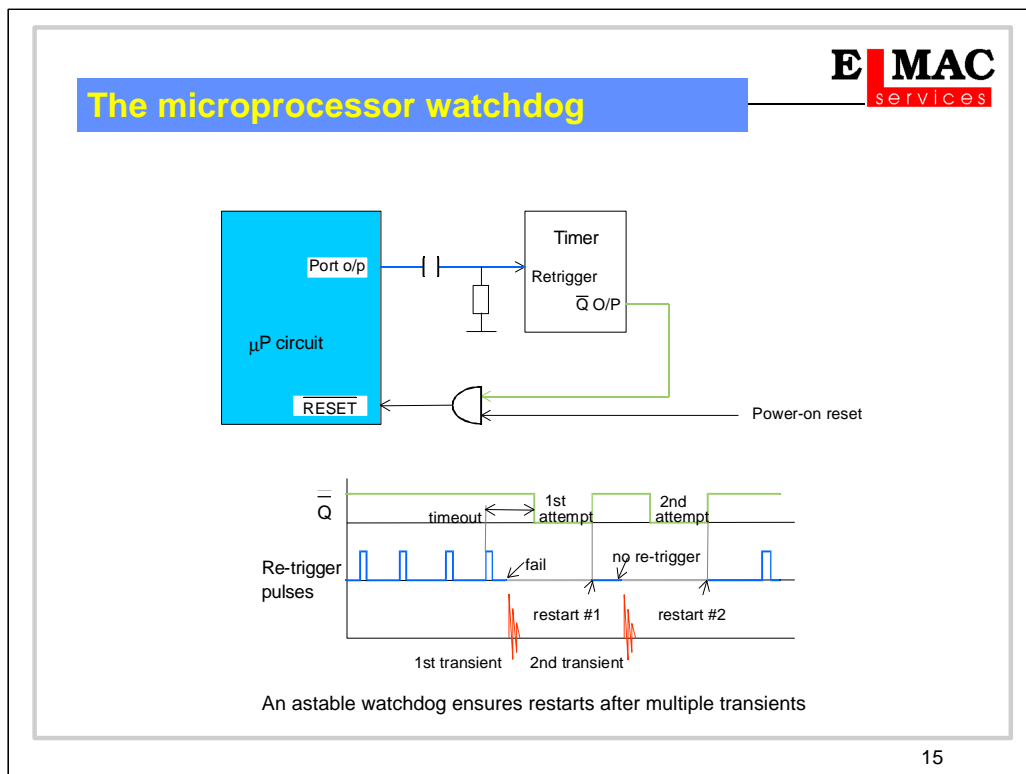
Local E- and H-fields induce voltages and currents into each logic node in the circuit. The level of interference voltage at each input will be a function of the circuit loop and node areas, and the circuit impedances. Minimizing the signal/OV geometry of each node, and choosing low output impedance drivers, will reduce the generated noise voltages, and using devices with a high static and dynamic noise immunity will maximize the threshold at which interference effects occur.

The first effect of RFI to be noticed on dynamically active logic circuits is timing jitter at the transitions. If the circuit timing is critical then this itself can cause maloperation. As the RF level increases then actual spurious logic level transitions occur and these will propagate through the circuit if the logic response speed is high enough. Usually, different thresholds are found for logic 0 and logic 1 effects because of the different driver output impedances. Clocked or edge-sensitive circuits will be particularly sensitive to transients as these will be latched asynchronously. Active high transition clock inputs are far more sensitive when held at logic 0 than when at logic 1.



Techniques to guard against corruption by transients and ESD are generally similar to those used to prevent RF emissions, and the same components will serve both purposes. Specific strategies aim to prevent incoming transient currents from flowing through the circuit, and instead to divert them harmlessly and directly to ground. To achieve this,

- keep all external interfaces physically near each other
- filter all interfaces to ground at their point of entry
- if this is not possible, isolate susceptible interfaces with a common-mode choke or opto-couplers
- use screened cable with the screen connected directly to ground
- screen pcbs from exposed metalwork with extra internally grounded plates



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The most serious result of a transient corruption is that the processor program counter, stack or address register is upset, so that it starts interpreting data or empty memory as valid instructions. This causes the processor to enter an endless loop, either doing nothing or performing a few meaningless operations. It will appear to be catatonic, in a state of "dynamic halt".

A watchdog guards against this by requiring the processor to execute a specific simple operation regularly, regardless of what else it is doing, on pain of consequent reset. A timer whose output is linked to the RESET input is itself being constantly retriggered by the operation the processor performs, normally writing to a spare output port. If the timer does not receive a "kick" from the output port for more than its timeout period, its output goes low and forces the microprocessor into reset.

If the interference transient recurs while the processor is re-booting it would be possible for a second crash to occur before the watchdog software had been re-enabled. For this reason it is important that the watchdog hardware should be capable of repeatedly restarting the processor until it succeeds. Also, the watchdog output should always be taken to the processor's reset input in order to ensure a correct re-start.

Defensive programming

- type-check and range-check all input data
- sample input data several times and either average it, for analogue data, or validate it, for digital data
- incorporate parity checking and data checksums in all data transmission
- protect data blocks in volatile memory with error detecting and correcting algorithms; implement write locking on non-volatile memory
- wherever possible rely on level- rather than edge-triggered interrupts; monitor the stack pointer for overflow
- periodically re-initialize programmable interface devices, especially I/O port registers
- incorporate token passing in subroutine calls

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Some precautions against interference can be taken in software, as noted above. Standard techniques of data validation and error correction should be widely used. Hardware performance can also be improved by software, particularly in ensuring that interference transients are distinguished from proper input data.

Some means of disabling software error-checking is necessary when testing equipment against interference, as otherwise the true performance of the hardware design cannot be assessed.

Not all microprocessor faults are due to interference. Other sources are intermittent connections, marginal hardware design, software bugs, meta-stability of asynchronous circuits, etc.

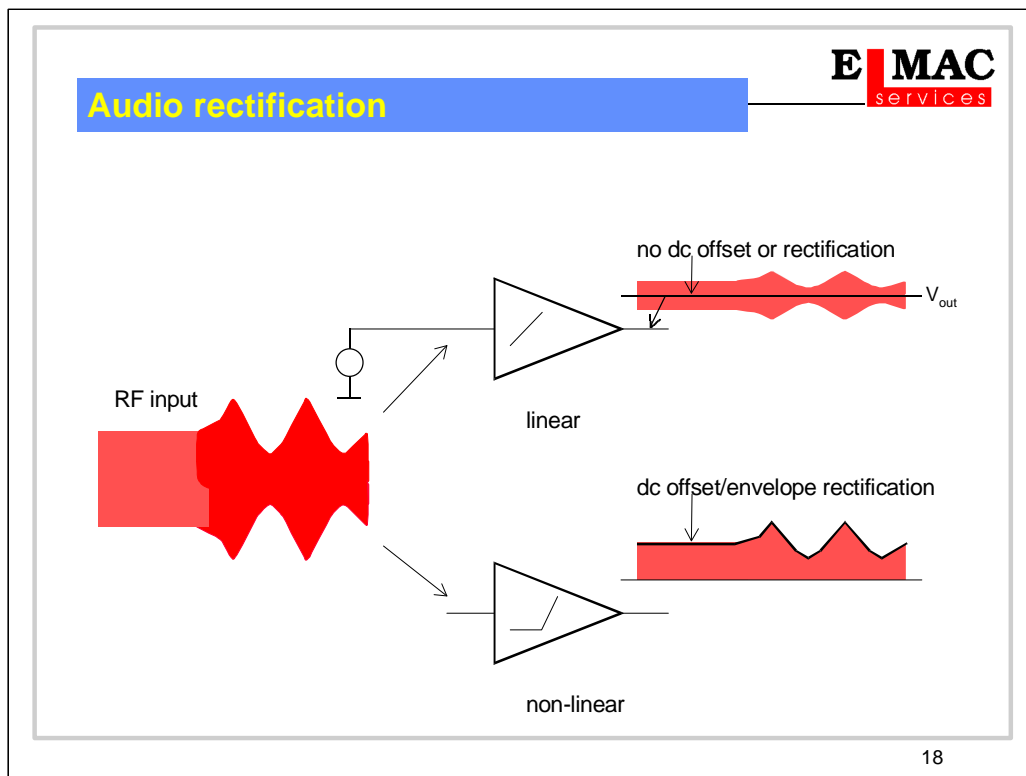
Analogue immunity design

- minimize circuit bandwidth and non-linearities
- maximize signal levels and dynamic range
- limit transient overload levels
- use balanced signal configurations
- isolate particularly susceptible paths

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RF interference within the signal frequency range is processed along with normal signals and is inseparable from them. In the case of frequency selective circuits such as PLLs or clocked ADCs there may be a narrowband response as the interfering frequency approaches the operating frequency, at which the circuit operation is completely disrupted. At other frequencies there is a worsening in signal-noise ratio, which may extend beyond the signal passband if the circuit bandwidth exceeds it. A circuit will be less sensitive to RF outside its passband but nonlinearities will create “audio rectification” and intermodulation products which may be within the signal passband.

Transient interference has in general less effect on analogue circuits than on digital. But transients may overload circuit functions (especially integrators) so that they become non-linear or fail to operate, and may then take a considerable time to recover, so that the duration of a transient's effect is much greater than its actual pulsewidth. Such effects are minimized by ensuring a high overload margin or by including overload suppression using appropriate clipping devices or other limiting circuits.



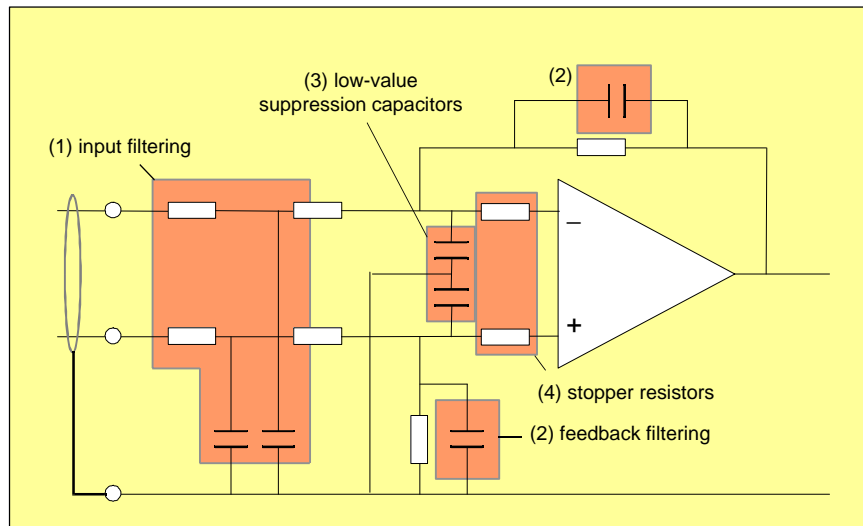
This is a term used rather loosely to describe the detection of RF signals by low-frequency circuits. It is responsible for most of the ill effects of RF susceptibility of both analogue and digital products.

When a circuit is fed an RF signal that is well outside its normal bandwidth, the circuit can respond either linearly or non-linearly. If the signal level is low enough for it to stay linear, it will pass from input to output without affecting the wanted signals or the circuit's operation.

If the level drives the circuit into non-linearity, then the envelope of the signal (perhaps severely distorted) will appear on the circuit's output. At this point it will be inseparable from the wanted signal and indeed the wanted signal will itself be affected by the circuit's forced non-linearity.

The response of the circuit depends on its linear dynamic range and on the level of the interfering signal.

Bandwidth, level and balance

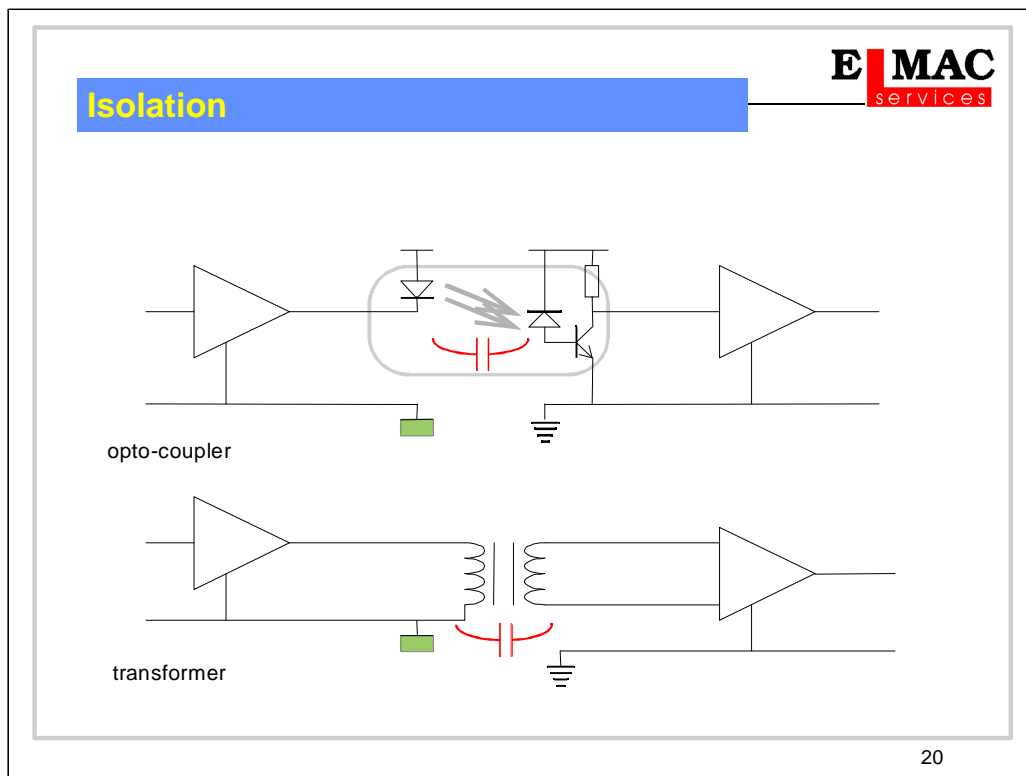


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Bandwidth should be restricted to the minimum acceptable by input RC or LC filtering (1), feedback RC filtering (2), and low value (10 - 33pF) capacitors directly at device terminals (3). Small capacitors directly across non-linear points, e.g. transistor base-emitter junctions, are especially helpful. Care should be taken with RC filters to ensure that they do not affect stability or worsen HF common-mode rejection. An even simpler method is to use low value stopper resistors or ferrites (4) at the inputs of all amplifying circuits.

Signal level should be maintained as high as possible throughout, consistent with other circuit constraints, in order to maximise the signal-to-induced-interference ratio.

Balanced circuit configurations take maximum advantage of the inherent common-mode rejection of op-amp circuits. But note that CMR is poorer at high frequencies and is affected by capacitive and layout imbalances. While balancing a circuit markedly improves its in-band interference immunity, it is less effective at improving RF and transient immunity.



Signals may be isolated at input or output with either an opto-coupler or a transformer, or in extreme circumstances by using fibre optic data transmission. Signal processing techniques may be needed to ensure accurate transmission of precision ac or dc signals, which increases the overall cost and board area.

Isolation breaks the electrical ground connection and therefore substantially removes common mode noise injection, as well as allowing a DC or low frequency AC potential difference to exist. However there is still a residual coupling capacitance which will compromise the isolation at high frequencies or high rates of dv/dt . This capacitance is around 1 - 2pF per device; where several channels are isolated the overall coupling capacitance (from one ground to the other) can rise to several tens of pF. Electrostatic screening reduces the signal coupling capacitance but not the common-mode capacitance. It is best to minimize the number of channels by using serial rather than parallel data transmission. Do not compromise the isolation by running tracks from one circuit near to tracks from the other.

End of this section