

PCB layout

Section 5

Outline

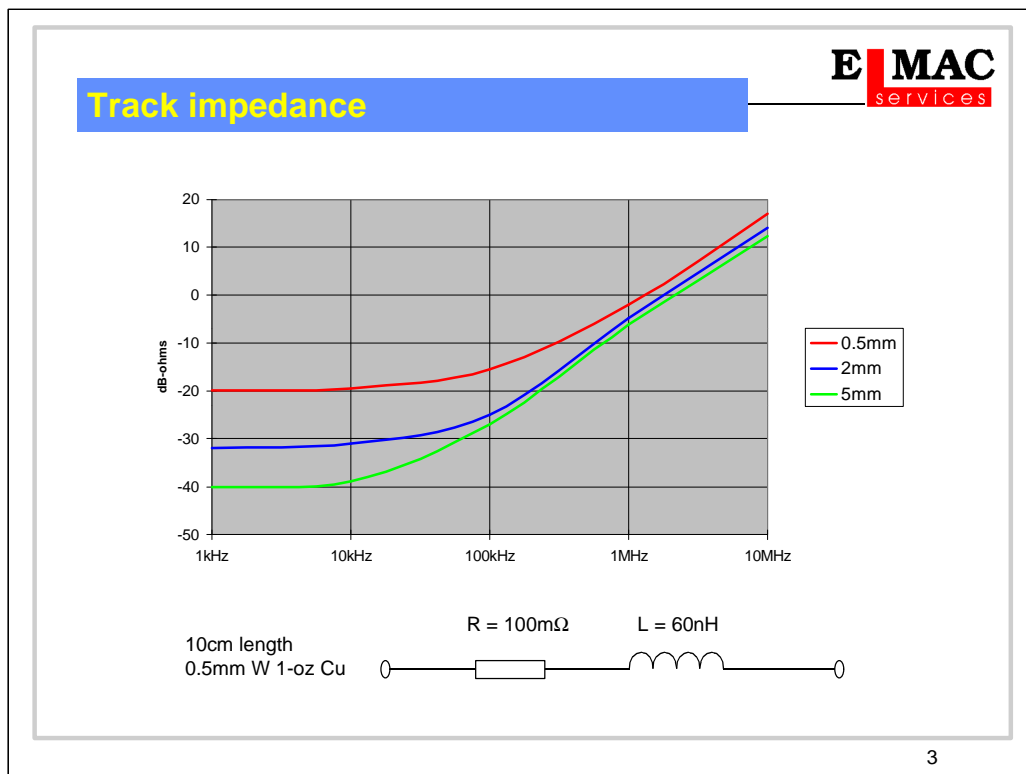


- grounding and track impedance
- proximity of return path
- gridded and ground plane layouts
- on-board shielding
- interface layout and grounding

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The way that a circuit is laid out on a pc board is critical to its EMC performance. Each track must be regarded as a component in its own right at high frequency. It is dangerous to delegate this aspect of design to a layout draughtsman who has little appreciation of the high frequency implications of layout and track routing choices, or worse, to an auto-routing CAD package which is totally ignorant of such aspects. Indeed, many auto-routers treat the circuit ground as a single node and must be specifically disabled in order to lay out the ground tracks properly.

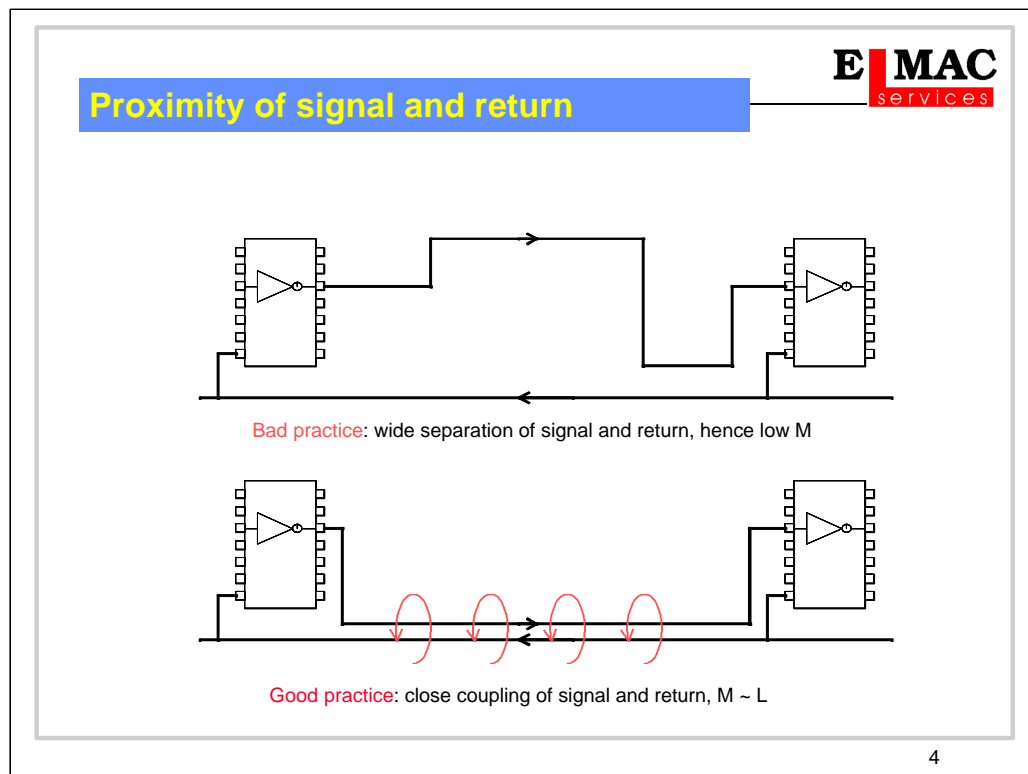
Proper PCB layout should be regarded as an integral aspect of circuit design and should start with the ground return tracks (or ground plane). These tracks should be laid first, continuing on to critical signal tracks such as those carrying high frequency clocks, data backplanes or especially sensitive circuit nodes. All of these tracks should be laid out to minimize their overall length and to minimize the area enclosed between them and their associated ground return path. Finally, the least sensitive or emissive circuits can be routed in the remaining available space.



Track impedance (that is, the end-to-end impedance of a length of track - not the same thing as transfer impedance Z_T or characteristic impedance Z_0) is dominated by inductance at frequencies higher than a few kHz. The inductance of a pcb track is primarily a function of its length, and only secondarily a function of its width. For a single track of width w and height h over a ground plane,

$$L = 0.005 \cdot \ln(2\pi \cdot h/w) \text{ microhenries per inch}$$

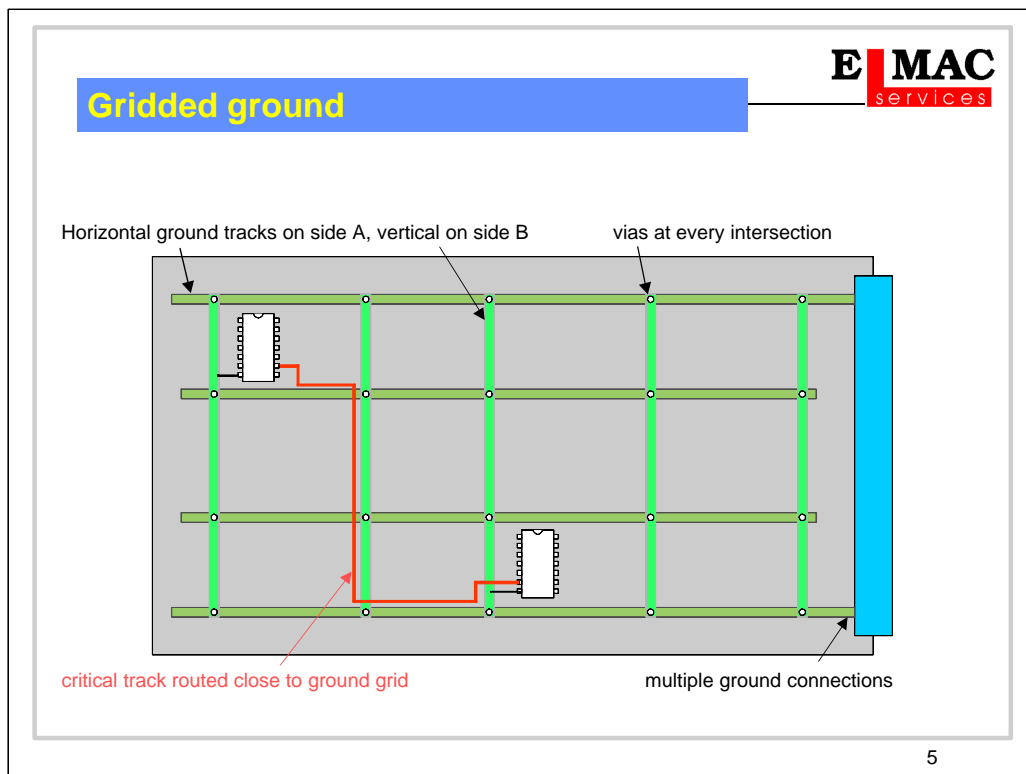
An overriding consideration for any track which will carry high frequencies at high currents is that it should be as short and direct as possible. The major factor in high-frequency impedance either of pc tracks or of wires is their length. Width, thickness or diameter are secondary factors.



Running signal and ground return tracks close together - so that the current flows in opposite directions - will reduce the ground impedance by a factor equivalent to the mutual inductance.

$$L_{\text{eff}} = 2(L - M)$$

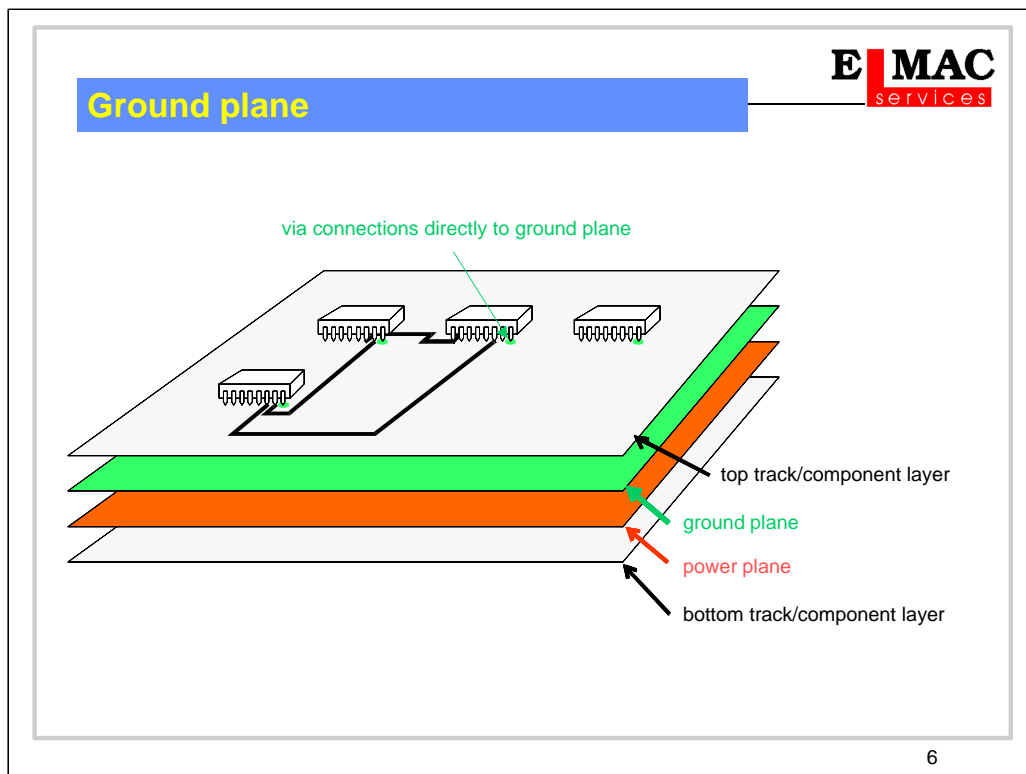
This effect is critical to understanding PCB track routing at radio frequencies. Knowledge of the ground current return path is essential. Given this, keeping the signal and ground paths adjacent along their length – and therefore *maximizing* their mutual inductance – will ensure not only minimum coupling with the magnetic fields around the pcb, but also minimum impedance of the return path and therefore minimum noise voltage developed *along* it. This will keep down the “noisiness” of the whole board, which is mostly responsible for common mode emissions, and will also improve its immunity to external interference.



A simple way to provide several parallel ground tracks is to form the ground layout in a grid structure. This maximizes the number of different paths that ground return current can take and therefore minimizes the ground inductance for any given signal route.

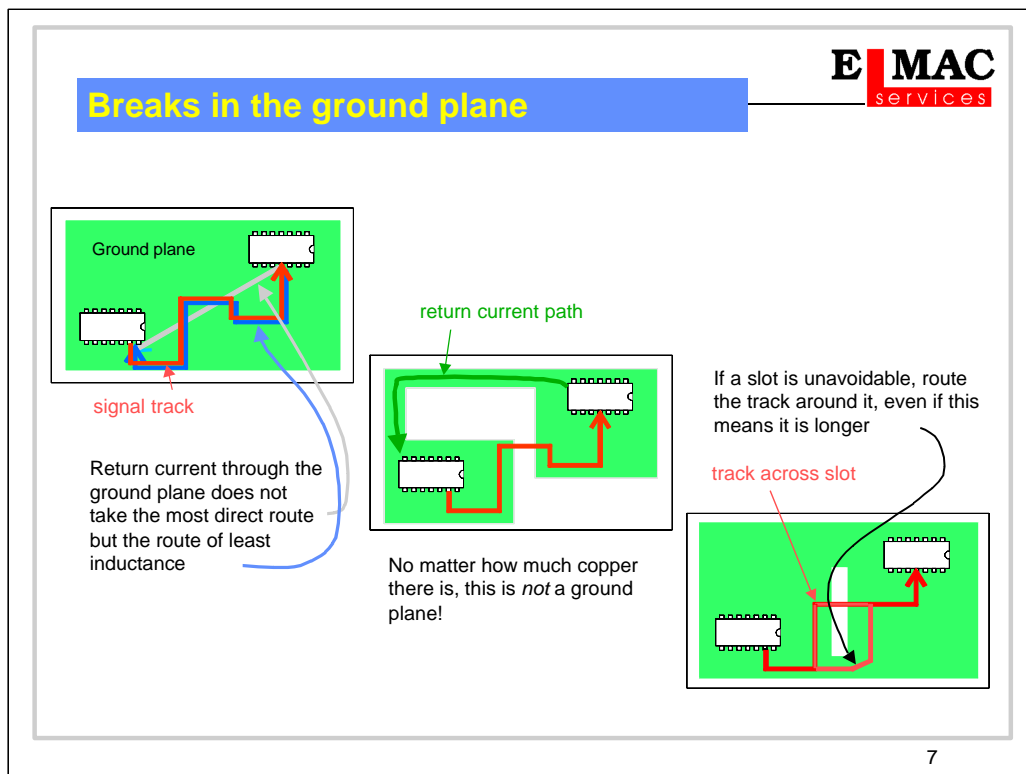
Such a structure is well suited to low speed digital layout with many packages, when individual signal/return paths are too complex to define easily. A wide ground track is preferred to narrow for minimum inductance, but even a narrow track linking two widely-separated points is better than none.

The grid layout is best achieved by putting the grid structure down first, before the signal or power tracks are laid out. Offensive (high di/dt) signal tracks can then be laid close to the ground tracks to keep the overall loop area small. With double-sided boards, the opposite sides can carry ground tracks in orthogonal orientations, with via connections at each intersection. As an extra precaution, dedicated ground tracks can be laid alongside offensive tracks.



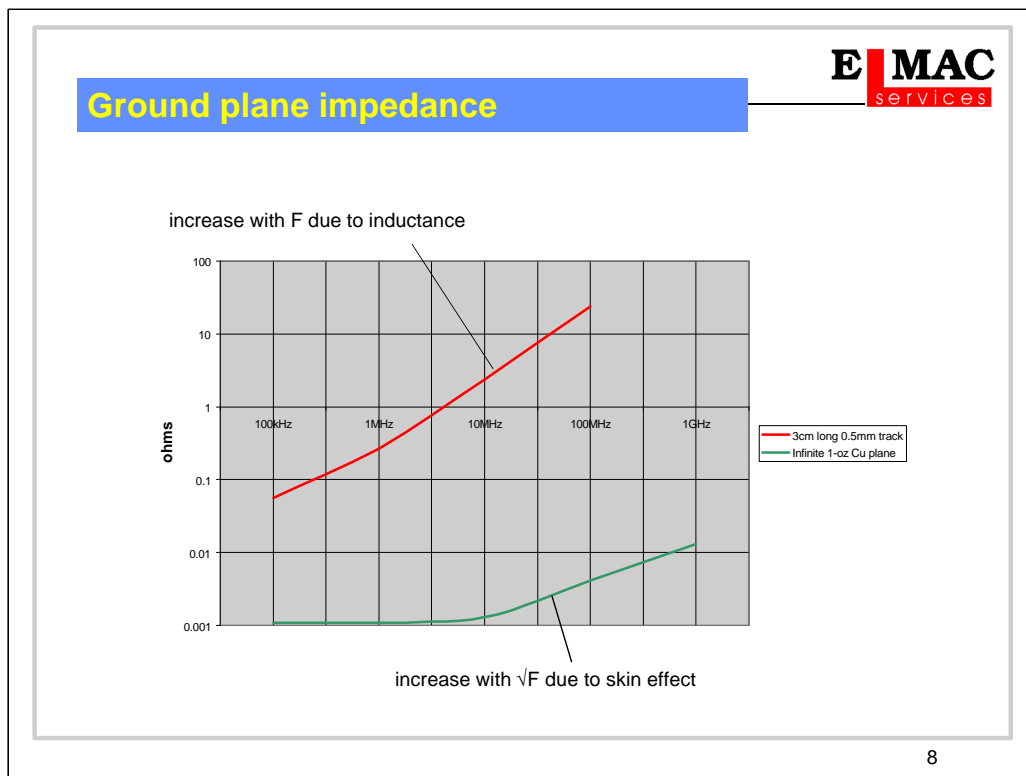
The lowest ground impedance is when an infinite number of parallel paths are provided and the ground conductor is continuous, and it is then known as a ground plane. This is easy to realize with a multilayer board and offers the lowest possible ground path inductance. It is essential for RF circuits and digital circuits with high clock speeds. The usual multilayer configuration also includes the power supply rail as a separate plane, which provides a low distributed source impedance for high frequency power supply currents. It also offers a defined characteristic impedance for signal tracks.

The ground plane will reduce mutual inductance coupling between circuits by ensuring that the coupled current loops are not co-planar. Capacitive coupling between tracks will not be directly affected by the ground plane, but the lowered impedance of each line may reduce capacitive crosstalk amplitude. The ground plane does provide a useful capacitive shielding effect between adjacent cards.



A partial ground plane is also possible on double-sided pcbs. At high frequencies, return current will flow preferentially in the neighbourhood of its signal trace. This is because such a route encloses the least area and hence has the lowest overall inductance. Thus the use of an overall ground plane ensures that the optimum return path is always available, allowing the circuit to achieve minimum radiating loop area by its own devices.

Not all of the copper area of a complete ground plane needs to be used, but edge effects will limit the effectiveness of a "partial" plane. What is essential is that the plane remains *unbroken* in the direction of current flow. If this is impossible it is preferable to include a small bridging track to link two adjacent areas of plane, but multilayer boards normally avoid the problem. A slot in the ground plane will nullify the beneficial effect of the plane if it interrupts the current, however narrow it is. If slots are necessary, critical tracks should be routed around the edge of the slot rather than directly across it. Large numbers of vias can create a slot in a multilayer construction and they should be broken into smaller groups to allow current flow in the plane between them.



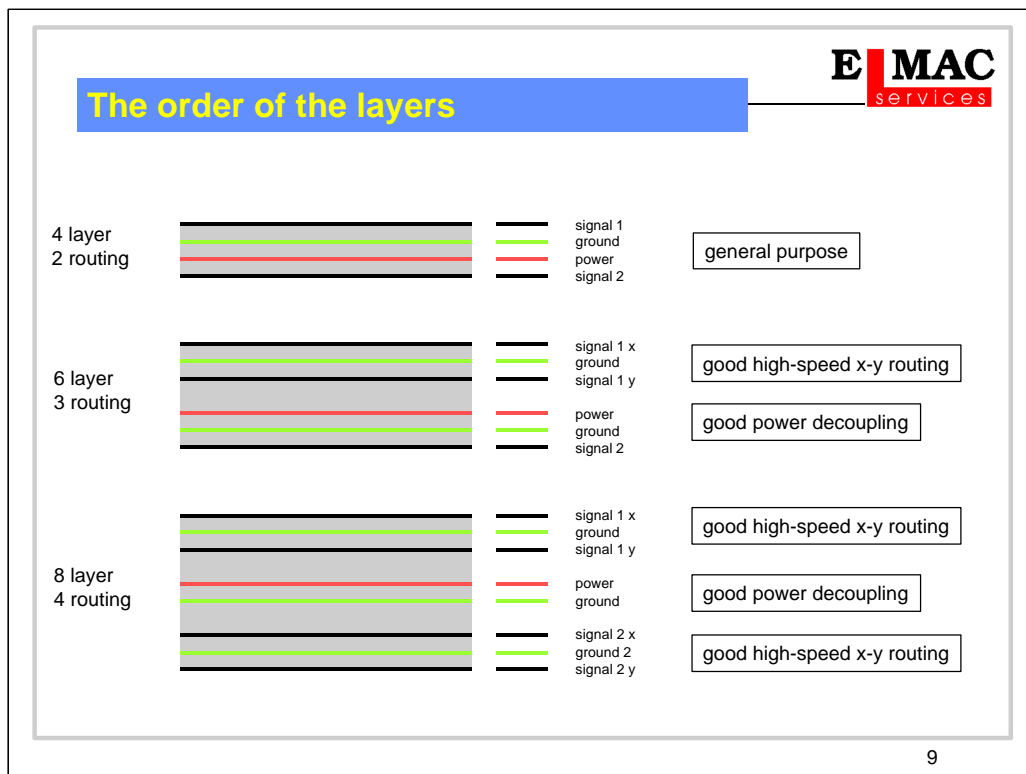
The effect of an *infinite* ground plane is to significantly reduce the common circuit ground impedance Z_G , by between 40 - 70dB, with respect to a single track. The actual improvement in circuit effect is not as great as the improvement in impedance because the return current spreads out to some extent from directly underneath the signal track.

As we have already seen, the impedance of a single track is dominated by inductance and increases linearly with frequency above a few tens of kHz. The infinite ground plane has no inductance and so at low frequencies the impedance is purely resistive and depends on the bulk resistivity of the material. However, the *skin effect* does play a role as frequency increases. This is a phenomenon in which current is crowded towards the surface of the conductor by the magnetic field distribution due to that current. The result is that less bulk conductor is available to carry the current at higher frequencies and so the effective impedance rises, but proportionally to the *square root* of frequency.

Real ground planes are not infinite in extent and the ideal impedance is not realised except at the centre of the board. Towards the edges the impedance rises. For this reason it is not advisable to locate noisy or sensitive components near the edge of the plane but to allow a rule of thumb distance of 10 times the layer thickness, at least, for such circuits (including their tracks) away from the edge.

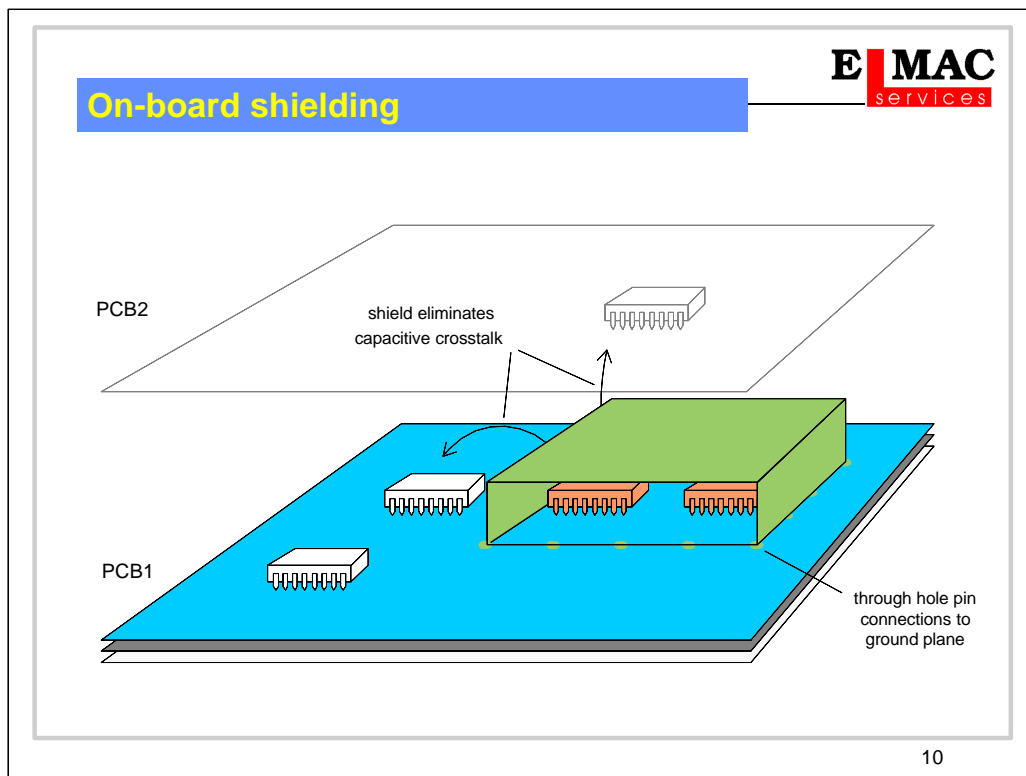
The skin depth in a conductor (the distance from the surface within which the current density has decreased by a factor of 8.6dB, or $1/e$) is given by

$$\delta = 1/\sqrt{\pi \cdot F \cdot \mu \cdot \sigma} \text{ metres}$$



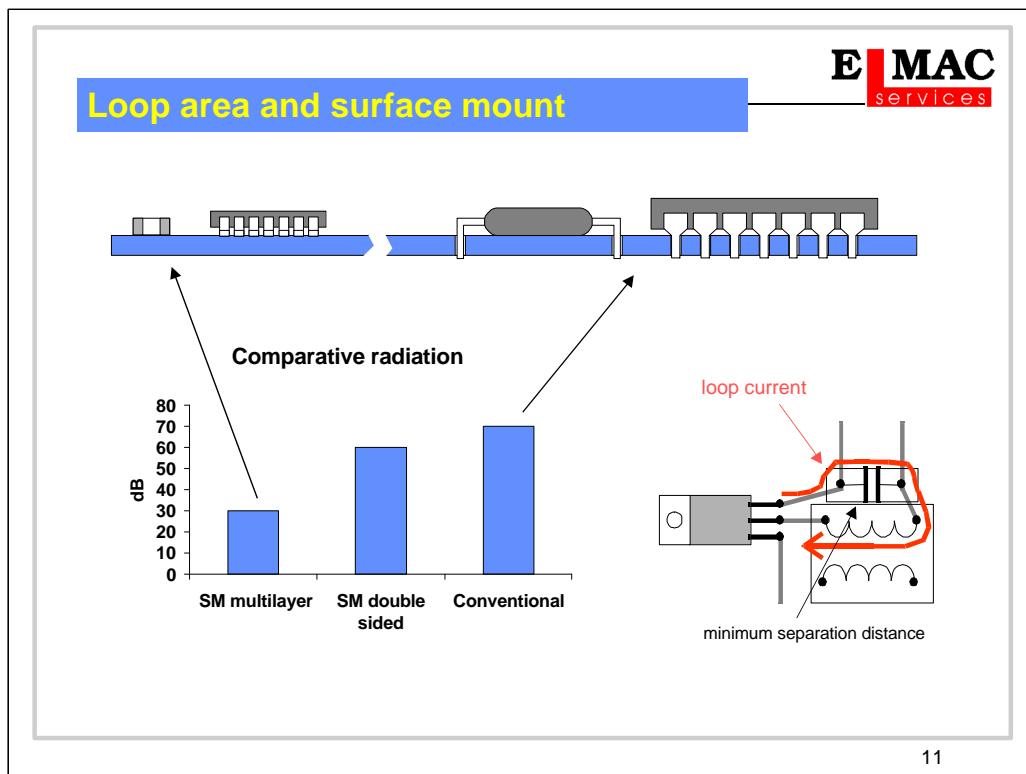
Note that the main EMC purpose of a ground plane is to provide a low- impedance ground and power return path to minimize induced ground noise. Shielding effects on signal tracks are secondary. Putting power and ground planes *outside* the signal planes on multilayer boards will only be a significant advantage if E-field shielding of the tracks is necessary, and this will in any case be compromised by the unavoidable fields from the components.

In multilayer (>4) configurations, the most important aspect is that every signal layer should be adjacent to a ground or power plane layer. Also, power and ground planes should be on adjacent layers to take advantage of the interlayer capacitance for high frequency decoupling. Critical tracks should be routed adjacent to ground rather than power planes, for preference. Such tracks (typically carrying high di/dt signals such as clocks) should also not jump through vias from one ground reference layer to another, unless the ground layers are tied together with vias at that point.



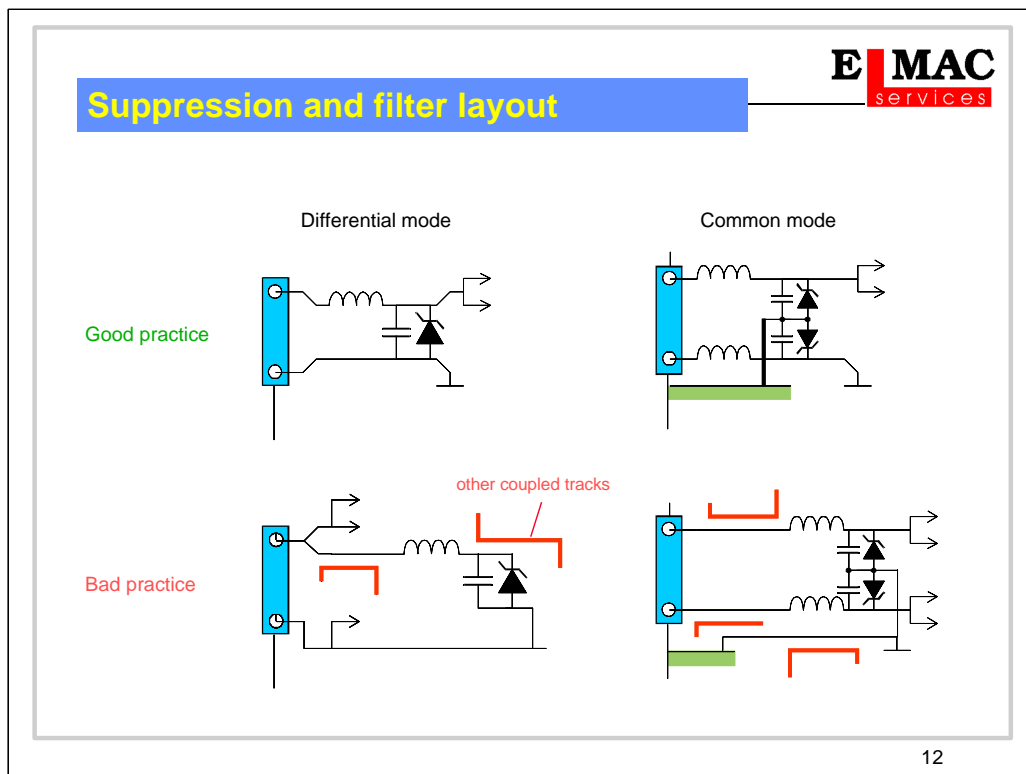
A shield can be placed around a particularly sensitive or noisy section of the circuit board. It can be constructed from thin pressed or electroformed sheet metal such as tinplate, and soldered via pins into the ground plane or connected via finger strip.

The major function of such an on-board shield is to minimize capacitive coupling to other parts of the circuit, including interface circuits which couple directly to the external environment. If used in this way, it is important that it is connected to a point of low RF noise voltage as otherwise the greater surface area and hence larger capacitance can actually increase coupling to other parts. It will shield against radiated fields provided that it forms a good Faraday cage with the PCB ground plane, i.e. there is near-continuous contact across the joint (solder pins spaced close together) and there are no appreciable apertures or seams in the shield. It may also be used as a low inductance local ground reference for decoupling purposes if a PCB ground plane doesn't exist. Tracks which exit from the shielded area may have to be filtered or decoupled to prevent noise from bypassing the shield.



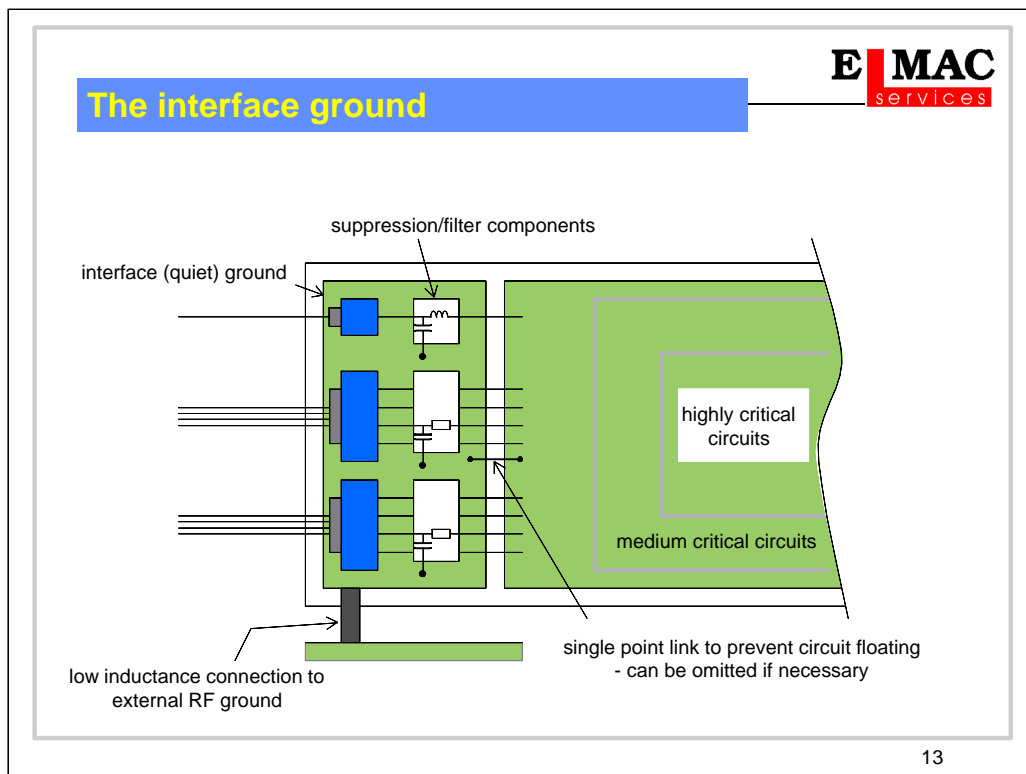
The goal of minimum loop area for signal and ground returns is aided by the use of surface mount components. A simple change from through-hole to SM components will reduce coupling by around 10dB simply because of the smaller dimensions of the board. But if this is added to the use of a multilayer PCB with ground and power planes, a much greater improvement is possible, because the smaller dimensions due to SM components are reinforced by the much smaller track loop areas possible by running tracks close to their planes.

For any circuit that includes a high di/dt path, the layout of the components which make up this path should be prioritised to make sure they are close together so that the loop area of this path is minimised.



Protection of the interfaces is a vital part of EMC. Normally LC or RC filters, perhaps in combination with transient suppressors, are used. These must be positioned immediately adjacent to the interfaces they are protecting, with short, direct tracks to the interface connector, not allowing any tracks between the protection and the connector to couple by inductive, capacitive or common impedance paths to other tracks on the board. With incoming frequencies up to 1GHz and transient rise times of the order of 1ns, only an inch or two of track may have a critical effect if it is poorly laid out.

Differential mode filtering is easily arranged by placing the filter components directly across the signal and return or power and return terminals. Common mode filtering needs more thought since the filter components must be referred to a “clean” ground reference plane, which will not normally be circuit 0V although it may be electrically tied to it at some point.



To prevent incoming interference (RF, transients, ESD) from propagating through the digital circuit ground tracks and corrupting the digital operation, the I/O cables should be grouped together and the circuit ground should if necessary be taken to the case at this point only. This also ensures that common-mode noise present on the digital ground is not fed out onto the cables. Decoupling and shielding techniques to reduce common-mode currents appearing on cables both require a “clean” ground point, not contaminated by internally generated noise. *Filtering at high frequencies is next to useless without such a ground.* The critical parameters for this “quiet ground” are that it should:

- provide a decoupling termination for all off-board connections, including the power supply;
- be referenced to the RF ground of the unit, either the chassis or a ground plate;
- not have circuit currents flowing in it.

These requirements can be ensured by devoting an area along one edge of the pcb to the quiet ground plane, including the I/O resistive, capacitive and inductive filtering and suppression elements on it (but no other circuits), and separating the circuit 0V from it either absolutely, or by a single connecting link. RF-critical circuitry should be widely separated from the I/O area. The quiet ground plane itself should be strapped to the chassis ground by one or more low-inductance links, e.g. the mounting pillars of the pcb.

