Design of Class E Amplifier With Nonlinear and Linear Shunt Capacitances for Any Duty Cycle

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***Abstract*—One of the main advantages of class E amplifiers for RF and microwave applications relies on the inclusion of a shunt capacitance in the tuned output network. At high frequencies, this capacitance is mainly provided by the output parasitic capacitance of the device with perhaps a linear external one for fine adjustments. The device's output capacitance is nonlinear and this influences the design parameters, frequency limit of operation, and performance of the class E amplifier. This paper presents a design method for the class E amplifier with shunt capacitance combining a nonlinear and linear one for any duty cycle, any capacitance's nonlinear dependence parameters, and any loaded quality factor of the tuned network. Nonlinear design with possibly different duty cycles is of relevance to maximize power or, alternatively, frequency utilization of a given device. Experimental, simulated, and compared results are presented to prove this design procedure.**

***Index Terms*—Class E amplifier, duty cycle, high efficiency, nonlinear shunt capacitance, RF power.**

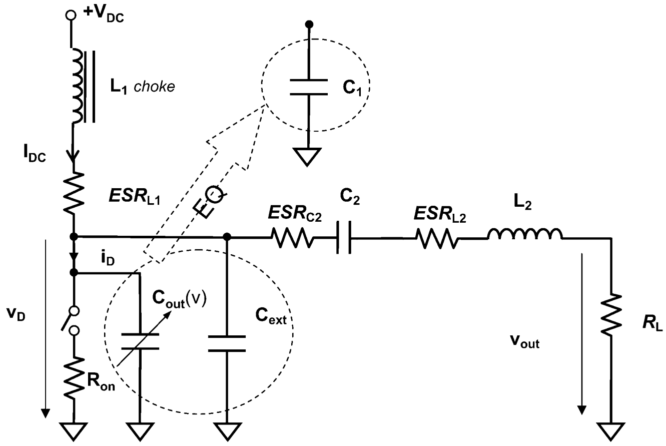

Fig. 1. Class E resonant tuned circuit with losses.

I. Introduction

CLASS E amplifiers [1] are advantageous networks for high-efficiency RF amplifiers because of the inclusion in the output tuned network of a capacitor shunting the device (C_1). As frequency increases, the parasitic capacitance of the device dominates the shunt capacitance. This capacitance is nonlinear and can be expressed by[1]

$$C_{\text{out}}(v) = \frac{C_{jo}}{\left(1 + \dfrac{v}{V_{\text{bi}}}\right)^n} \tag{1}$$

with C_{jo} being the capacitance at zero voltage, V_{bi} being the built-in potential (generally ranging from 0.5 to 0.9), and n being the grading coefficient of the pn-junction.

Several authors acknowledge the importance of designing class E amplifiers taking into account this nonlinear capacitance, and a few approaches have been published. The analytical solution for a restricted set of conditions was started by Chudobiak in [2] for $n = 0.5$ and duty cycle was also 0.5. A more practical example with similar restrictions is presented in [3] and further discussed in [4], allowing combinations of linear and nonlinear shunt capacitances, something already seen in [5]. Numerical approaches expand the method for a variety of grading coefficients and several other more realistic situations [6], [7], but the degree of freedom presented in this paper is novel.

This method is based on the computation of an equivalent linear capacitance C_{eq} of the device's nonlinear one, as defined in [8] and [9]. The linear equivalent includes both the linear external capacitor and the nonlinear parasitic contribution. As a consequence of this definition, the frequency limit of the amplifier can be improved [10], [11]. The advantage of such a capacitance is the ability to account for the nonlinearities in classical designs by mere substitution of C_1 with the equivalent value, except for some effects (such as the maximum drain peak voltage) that are recalculated. The form factor α is defined to describe the role played by the nonlinear counterpart in C_{eq}.

In this paper, we present a class E design method for the circuit depicted in Fig. 1, including the nonlinear output capacitance of the device, valid under the following conditions.

Condition 1) Any duty cycle. This is important because for a given device and frequency of operation, maximum output power may be obtained at a different duty cycle than 50%. Additionally, to maximize the frequency of a device in class E for a given output power, optimum D is 33% [10].

Condition 2) Efficiency is 100%, thus, the zero-voltage-switching (ZVS) $v_D(2\pi) = 0$ condition is satisfied, but the zero-voltage-derivative-switching (ZVDS) condition $(dv_D/dt(2\pi) = 0)$ is not mandatory (if satisfied,

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[1]Although this work is primarily aimed at power MOSFETs, analysis may be applied to other microwave devices such as MESFETs, HBTs, pseudomorphic HEMTs (pHEMTs), etc.

optimum operating conditions will occur, if not, nominal switching conditions). Losses in all the network components and in the device may also be considered, in which case, η will not be 100%. Losses are accounted for in the performance, but not modifying the design values of the class E components.

Condition 3) The built-in potential $V_{\rm bi}$ and the grading coefficient n in (1) are not fixed and can be chosen by the designer. Guidelines on how to obtain them are provided.

Condition 4) Loaded quality factor of the tuned output network is not necessarily high and, again, can be chosen by the designer.

The resulting circuit parameters and performance of the class E amplifier are numerically obtained. A good number of representative results are presented graphically and in tables. To prove this method, three different verification approaches are included.

II. Equivalent Capacitance and Form Factor

Utilizing the nonlinear description of the capacitance in a completely analytical description of the class E amplifier has proven unfeasible unless a good number of constraints are imposed in the assumptions.

The equivalent capacitance [8] $C_{\rm eq}$ obtained and used in this paper is specifically defined as *the constant (thus, linear) capacitance that substituted for the nonlinear intrinsic capacitance $C_{\rm out}(v)$ produces the same nominal operating conditions (ZVS) at the instant of turn on that would occur with the real device's capacitance, maintaining the values of the rest of the amplifier's elements*. Such a linear equivalent is also used in [3], but in this case, the ZVDS condition is always assumed, which is a more particular case of the one used here.[2]

With this definition, classical design methods may be used, substituting the nonlinear capacitance for its equivalent one. Nevertheless, and even though the equivalent capacitance yields the same switching conditions as the real capacitance, the voltage waveform across the device with a nonlinear capacitance is different during the OFF interval. The nonlinear nature of the capacitance increases the voltage peak across the device, even though the switching occurs under the same conditions and at the same instant. The increase factor depends on the fraction of the total capacitance that is provided by the device. This detail has to be taken into account by designers to select transistors with a higher breakdown voltage in order to maintain safe operating conditions for the amplifier and to protect the circuit from over-voltages due to nonlinearities. The design method presented in this paper provides the new peak voltage value normalized by the supply voltage.

To quantify the percentage of nonlinearity in C_1, we define the form factor α as the quotient of the equivalent capacitance $C_{\rm eq}$ and the theoretical value of C_1

$$\alpha = \frac{C_{\rm eq}}{C_1} \tag{2}$$

[2]This analysis could also be restricted to include the condition of zero voltage derivative at turn on and, therefore, calculate the optimum linear equivalent capacitance. On the other hand, the nominal operating mode has been adopted in order to achieve greater generality.

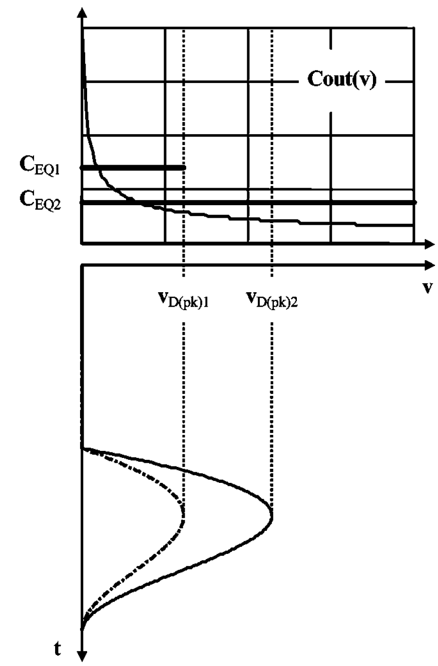


Fig. 2. Equivalent capacitance with two different supply voltages.

with

$$C_1 = C_{\rm eq} + C_{\rm ext} \tag{3}$$

where $\alpha = 0$, C_1 is completely linear (classical analysis is completely valid). If $\alpha = 1$, it means that C_1 is completely produced by $C_{\rm eq}$; i.e., $C_{\rm ext}$ equals zero and $C_{\rm out}(v)$ provides the whole necessary C_1. To estimate the equivalent capacitance, it is necessary to know the device's output capacitance response [see (1)], in this sense, every single parameter influencing $v_D(t)$ would also influence $C_{\rm out}(v)$; therefore, the supply voltage and the form factor play a relevant role in $C_{\rm out}(v)$. Mathematically,

$$C_{\rm eq} = f(C_{jo}, n, V_{\rm bi}, V_{\rm DC}, \alpha). \tag{4}$$

A. Supply Voltage Influence on $C_{\rm eq}$

According to the mathematical model chosen to represent the voltage dependence of $C_{\rm out}(v)$, the higher the supply voltage $V_{\rm DC}$, the lower the equivalent capacitance because $C_{\rm out}(v)$ will reach lower values due to broader voltage excursions. In Fig. 2, two operating situations have been plotted with two different supplies, i.e., $V_{\rm DC1}$ and $V_{\rm DC2}$, each one leading to a different voltage waveform and to a different peak voltage ($v_{D(pk)1}$ and $v_{D(pk)2}$). The excursion to a higher voltage value in the second case yields a reduction in the equivalent capacitance value.

B. Form Factor α Influence on $C_{\rm eq}$

The equivalent capacitance also depends on the contribution of the nonlinear capacitance to the total required capacitance C_1. This contribution is exactly what is characterized by the form factor α. Thus, the higher the value of α (the closer it is to unity), the greater the influence of the nonlinearities and, therefore, the higher the voltage peak across the device. The equivalent capacitance increases at the same rate as the contribution

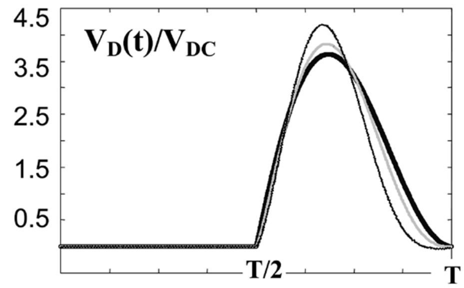


Fig. 3. Drain voltage waveform for three different form factors. $\alpha = 0.05$: solid line. $\alpha = 0.55$: gray line. $\alpha = 1$: dotted line.

TABLE I
CLASS E CIRCUIT VALUES FOR THREE DIFFERENT FORM FACTORS [10]

D	Q_L	$C_jo[pF]$	n	$V_{bi}[V]$	$V_{DC}[V]$
0.5	10.62	1000	0.4	0.65	20

	α	$f[MHz]$	$C_{eq}[pF]$
QUASI-LINEAR	0.05	0.1534	137.29
PARTIALLY NONLINEAR	0.555	1.2437	274.77
COMPLETELY NONLINEAR	1	2.0623	304.28

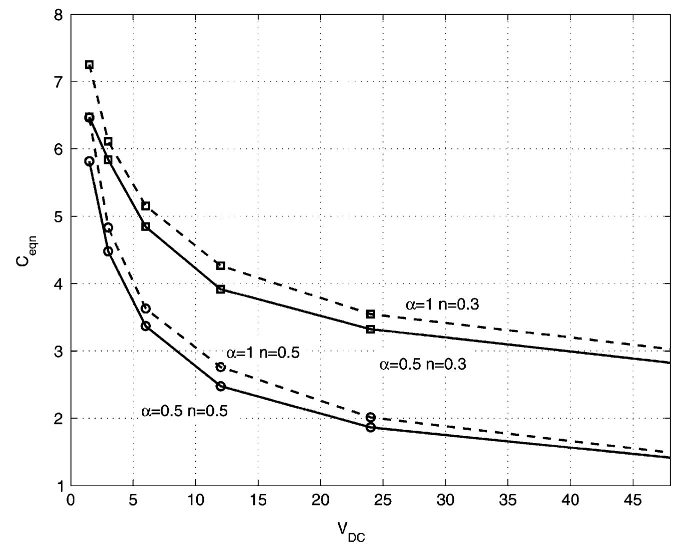


Fig. 4. Equivalent normalized capacitance $C_{\rm eqn}$ as a function of $V_{\rm DC}$ for $Q = 5$ and $D = 0.5$ for $\alpha = 0.5$ (solid line) and $\alpha = 1$ (dashed line), and for two different values of n: $n = 0.3(-\square-)$ and $n = 0.5(-\circ-)$. In all cases, $V_{\rm bi} = 0.6$.

of the device capacitance increases in relation to the total C_1. Fig. 3 illustrates three different responses of a class E amplifier with the same output nonlinear capacitance (e.g., the same device) and the same supply voltage, but at three different frequencies. At very low frequencies, 150 kHz in the example, the nonlinear device capacitance is a negligible part of the total capacitance and the linear capacitance dominates. On the other hand, at 2 MHz, the nonlinear device output capacitance dominates the total capacitance required for optimal class E operation. The actual values are given in Table I. The switching conditions remain the same, but the equivalent capacitances, the form factors, peak voltages, and waveforms are different.

C. Computing the Linear Equivalent Capacitance

To compute the equivalent capacitance, a numerical state-space description of the class E amplifier has been programmed, allowing for nonlinear capacitance and including losses in all the circuit elements [12]. To compute the equivalent capacitance, the algorithm comprises the following steps.

Step 1) First design a completely linear and ideal class E, obtaining a linear C_1 by means of classical results (e.g., [13]).

Step 2) Substitute the linear capacitance C_1 for a partially nonlinear one (thus, α needs to be known) and an external one. Change the nonlinearity constant C_{jo} and iterate until equivalent nominal switching conditions are obtained (ZVS). Alternatively, also include ZVDS for the optimum equivalent. To do this, n and $V_{\rm bi}$ have to been known. To estimate those values, use a reverse curve-fitting method, if any information of variation of output capacitance with voltage is provided in the datasheet, or obtain those values from measurements [14] if otherwise.

Step 3) This computed nonlinear capacitance will be the equivalent of the previous linear one. This equivalent capacitance is a function of the values of n, $V_{\rm bi}$, $V_{\rm DC}$, and α that have been considered.

For simplicity in this paper, a good number of equivalent capacitances have been computed and are presented in the tables included in the Appendix for a wide range of supply voltages and form factors and for several values of n and D. A clarifying explanation on how the computation of a $C_{\rm eq}$ integrates in the design process is provided in Section IV.

III. CIRCUIT ANALYSIS

The circuit of the class E amplifier analyzed is presented in Fig. 1. The derivation of the equations considers the following assumptions.

- The inductance of the choke coil L_1 is large enough so that current may be considered constant.
- The shunt capacitance is considered linear, but it consists of the linear equivalent of the nonlinear output capacitance and the external capacitor. Therewith, nonlinearities are taken into account.

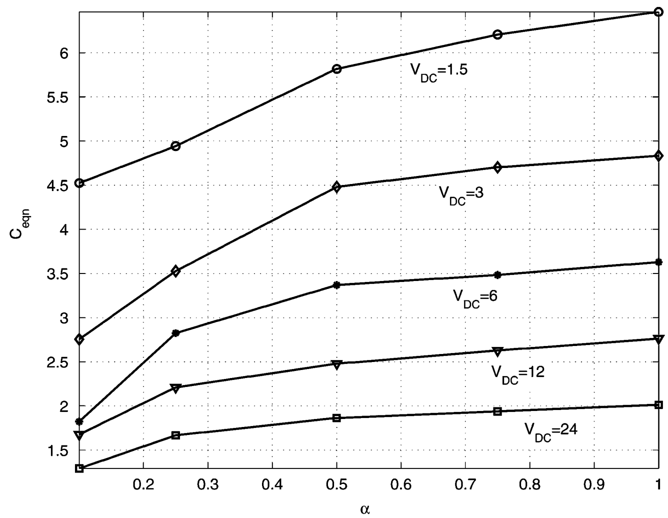
Let the starting point of this analysis be the amplifiers response constants [13], which are defined by

$$\frac{\omega \cdot L_2}{R_L} = K_1$$
$$\omega \cdot R_L \cdot C_2 = K_2$$
$$\omega \cdot R_L \cdot C_1 = K_3 = K \qquad (5)$$

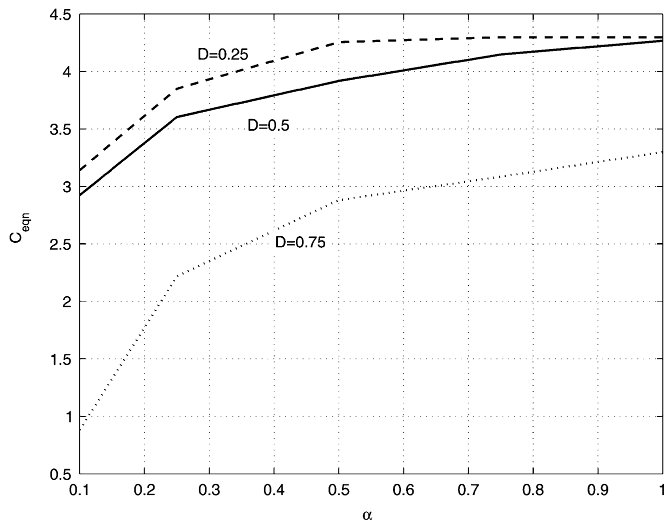
with C_1 from (3). The nominal operating waveforms of the amplifier depend on these constants. Thus, different circuit parameters of the output tuning network R_L, C_1, C_2, and L_2 yield the very same waveforms under nominal operating conditions if the preceding parameters K_1, K_2, and K remain constant. These amplifier response constants are Q and D dependent.

Substituting C_1 for (2),

$$2\pi \cdot f \cdot R_L \cdot \frac{C_{\rm eq}}{\alpha} = K(Q_1, D) \qquad (6)$$

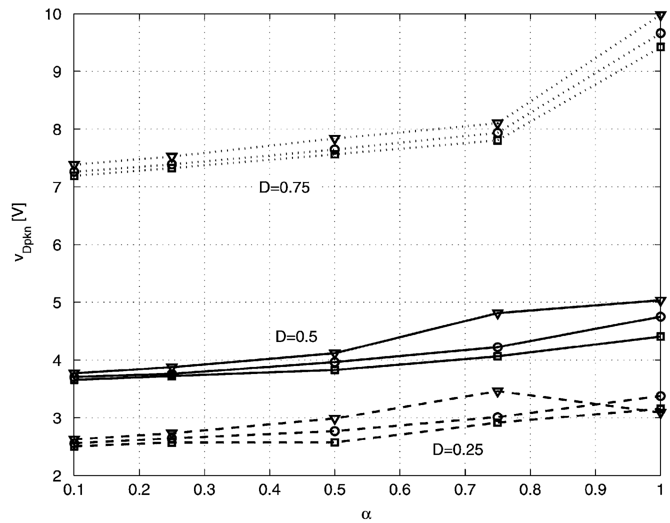


(a)

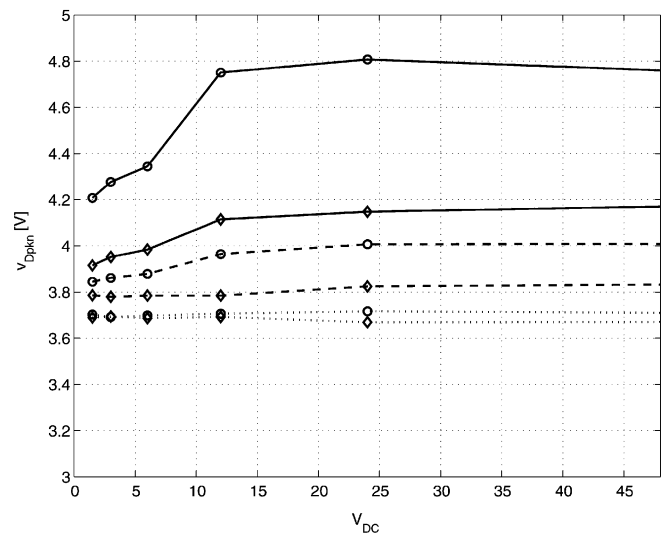


(b)

Fig. 5. Equivalent normalized capacitance C_{eqn} as a function of the form factor α for $Q = 5, V_{\mathrm{bi}} = 0.6$, and $n = 0.5$. (a) For several values of V_{DC}: $V_{\mathrm{DC}} = 1.5$ V $(-\circ-)$, $V_{\mathrm{DC}} = 3$ V $(-\diamond-)$, $V_{\mathrm{DC}} = 6$ V $(-*-)$, $V_{\mathrm{DC}} = 12$ V $(-\nabla-)$, $V_{\mathrm{DC}} = 24$ V $(-\Box-)$. In all these cases, $D = 0.5$. (b) Fixed supply voltage of 12 V and several duty cycles: $D = 0.25$ (dashed line), $D = 0.5$ (solid line), and $D = 0.75$ (dotted line).



(a)



(b)

Fig. 6. (a) Normalized drain peak voltage v_{pkn} as a function of α for $D = 0.25$ (dashed line), $D = 0.5$ (solid line), and $D = 0.75$ (dotted line) and for $Q = 2(-\nabla-)$, $Q = 5(-\circ-)$ and $Q = 10(-\Box-)$ for $V_{\mathrm{DC}} = 12$ V and for $n = 0.5$. (b) Normalized drain peak voltage v_{pkn} as a function of V_{DC} for the particular case of $D = 0.5$ and $Q = 5$ and for $\alpha = 1$ (solid line), $\alpha = 0.5$ (dashed line), and $\alpha = 0.1$ (dotted line) and for $n = 0.3(-\diamond-)$ and $n = 0.5(-\circ-)$. In all cases, $V_{\mathrm{bi}} = 0.6$.

with Q_1 being the loaded quality factor of the output network in conduction.[3]

A certain C_{eq} calculated for a particular amplifier with a specific load and operation frequency will still be valid for other cases provided that $\omega \cdot R_L \cdot C_1, \omega \cdot R_L \cdot C_2$ and $\omega \cdot L_2/R_L$ remain constant in all of them.

A. Parameter Normalization

A normalization of the equivalent capacitance by the factor C_{jo} proves very interesting because C_{jo} is a mere linear scaling factor in the characterization of the linear equivalent capacitance C_{eq} (1). Thus, the following normalization can be applied:

$$C_{\mathrm{eq}} = C_{jo} \cdot C_{\mathrm{eqn}}. \tag{7}$$

[3] $Q_1 = \omega_1 L_2/R_L$, where $\omega_1^2 = 1/(L_2 C_2)$. The expression may be related to $Q_L = \omega L_2/R_L$ [13].

Including this in (6),

$$2\pi \cdot f \cdot R_L \cdot C_{jo} \cdot \frac{C_{\mathrm{eqn}}}{\alpha} = K(Q_1, D). \tag{8}$$

In general, the normalizing equations can be defined as follows.

1) Normalized frequency

$$f_n = f \cdot R_L \cdot C_{jo}. \tag{9}$$

2) Normalized equivalent capacitance

$$C_{\mathrm{eqn}} = \frac{C_{\mathrm{eq}}}{C_{jo}}. \tag{10}$$

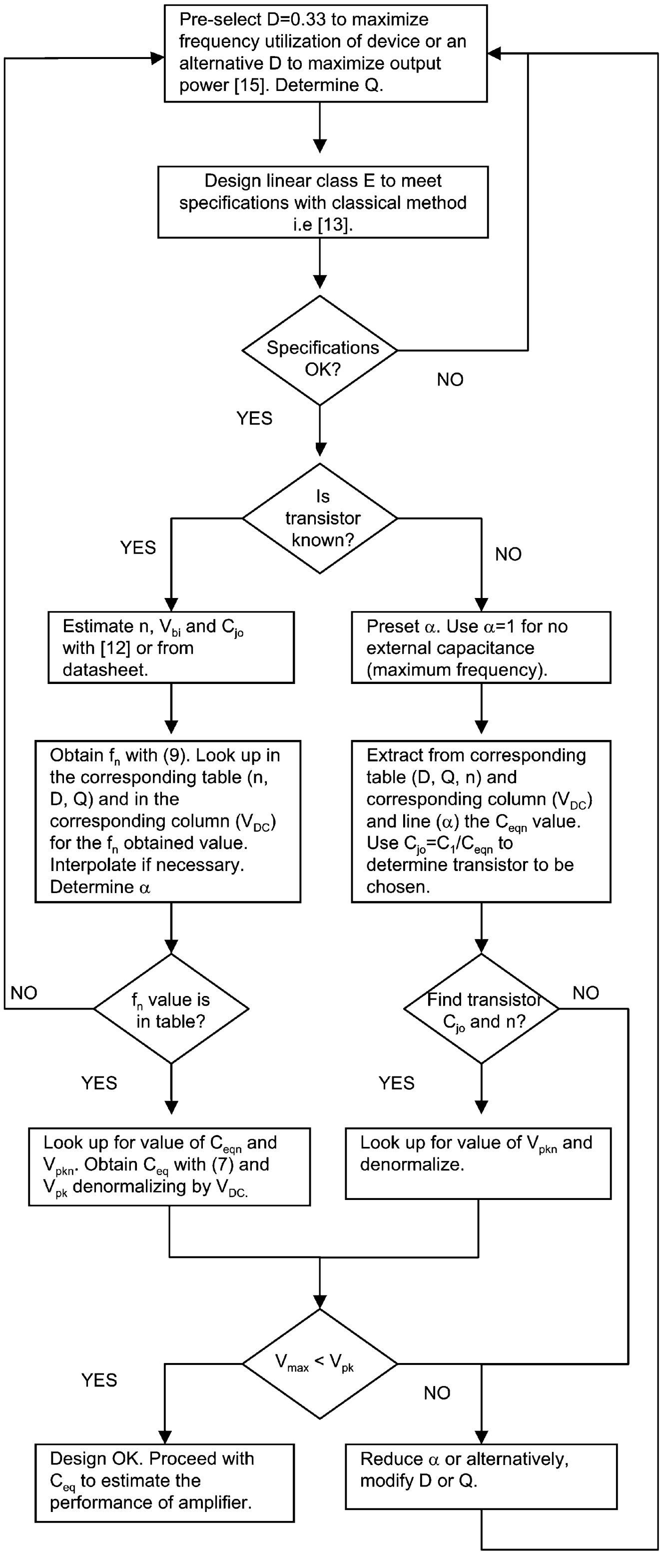


Fig. 7. Class E design process using numerical results in the tables. $V_{\max}$ is the maximum voltage withstood by the transistor (given by manufacturers in the datasheet).

By combining them all and substituting in (6), the following expression is obtained:

$$2\pi \cdot f_n \cdot \frac{C_{\text{eqn}}}{\alpha} = K(Q_1, D). \tag{11}$$

TABLE II
VERIFICATION BY COMPARISON WITH [4]

Specifications			
f	4MHz	D	0.5
V_{DD}	20V	Q	10
P_o	4W		
Circuit parameters obtained			
	In [4]		This method
	Theory	Experiment	
f	4MHz	3.91MHz	4MHz
R	57.5Ω	51Ω	57.68Ω
C_{ext}	40pF	20pF	60.4pF-C_{stray}
C_{eq}	Not calculated		87.75pF
L_2	22.9μH	23μH	22.95μH
C_2	79.4pF	77pF	78.306pF
$L_{1(MIN)}$	100μH	100μH	100μH
v_{Dpeak}	80.8 V	87.17V	79.691V
$v_{om_{load}}$	21.48V	22.51V	21.481V
η	-	91%	98%

NOTE: C_{stray} accounts for PCB parasitics or oscilloscope probe.

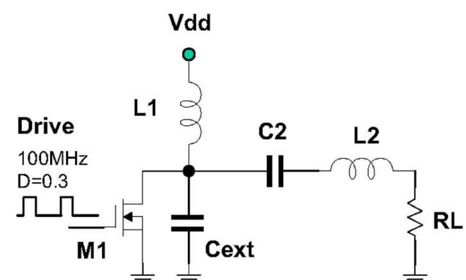


Fig. 8. Class E amplifier with losses built for experimental verification.

Maintaining K_1 and K_2 constant and solving the problem numerically for K leads to the results determining the design parameters. We have obtained a set of equations with a significant generality, provided that the values of K_1, K_2, and K remain constant. This is important because it makes the results independent of actual load resistance R_L and of C_{jo} (which depends on the exact member of a device family). The normalization might also be extended to voltage and current waveforms, defining the normalized voltage or current as the value of the voltage across or current through a node divided by the value of V_{DC} or I_{DC}, respectively. The normalized results of the numerical design method will be presented according to this nomenclature.

Some results are shown here in the form of graphs. In Fig. 4, the dependence of C_{eqn} with V_{DC} is shown for two different form factors and two different n values. The more linear the capacitance (lower α), the lower the equivalent capacitance. As n increases, the device's output capacitance also decreases and so does C_{eq}. Fig. 4 graphically shows the effect described in Section II-A, demonstrating that the higher the supply voltage, the lower the equivalent capacitance. Fig. 5(a) shows the dependence of C_{eqn} with α for several values of supply voltage. In Fig. 5(b), the same dependence is shown, but for three different duty cycles. Fig. 6(a) and (b) shows the results for the normalized peak voltage v_{pkn} as a function of α and V_{DC}, respectively. The first one shows that the peak varies strongly with the duty

TABLE III
SIMULATED AND EXPERIMENTAL VERIFICATION CIRCUIT

Design Parameters			
Device	PolyFET P123	f	100MHz
V_{DC}	16V	P_o	1W
D	0.3	Q	5
Circuit values			
	Theory	Simulation	Prototype
C_1	15pF	-	-
C_{ext}	-	8pF ($ESR@100MHz = 0.01\Omega$)	Probe setup (approx. 8pF)
C_{eq}	7.04pF $\alpha = 0.425$	-	-
R_{Lopt}	24Ω	16.2Ω	16.2Ω
L_1	600nH	538nH ($ESR@100MHz = 2.817\Omega$)	Coilcraft 132-20SM MaxiSpring
L_2	257.31nH	246nH ($ESR@100MHz = 1.2\Omega$)	Coilcraft 132-15SM MaxiSpring
C_2	17.86pF	18pF ($ESR@100MHz = 0.2\Omega$)	08051A180JA AVX USeries
Results			
	Theory	Simulation	Measured
$v_{Dpk}^{(1)}$	46.15V	42V	48.3V
v_{ompk}	5.63	5.1V	4.6V
η	72.7%	66%	71.4%

cycle and does not vary significantly with Q. In general, the peak voltage value is higher for increasingly nonlinear situations, as expected. Fig. 6(b) highlights that, except for very low values of supply voltage, the normalized peak value does not depend on the actual V_{DC} and the more nonlinear (higher form factor, higher n), the higher the peak.

IV. DESIGN PROCEDURE

Generally, the specifications of a class E amplifier are: frequency, intended output power, and available supply voltage, and sometimes also output harmonic content (Q_L). Generally, duty ratio is not predetermined by external conditions, although some constraints may apply depending on the available driver. If no external constraints apply, the idea is to select a duty cycle equal to 0.3 to maximize the frequency utilization of a device or, alternatively, use [15] to maximize output power depending on losses.

At this point, there are two possible lines of action. The first one is to use the tables that include numerical results in the Appendix. If the exact parameter values for D, Q or V_{DC} are not listed in them, interpolating values are still applicable with good results. How to design a class E amplifier using this method is summarized in the flowchart of Fig. 7. Secondly, if the parameter values are very different to those in the tables, or high accuracy needs to be achieved, additional numerical results need to be obtained and the method needs to be numerically programmed. To do so, the following steps apply.

Step 1) Calculate C_{eq} with the method proposed in Section II-C. Iterate for a good number of α values and some possible variation of V_{DC} depending on constraints. Obtain C_{eqn} with (10). This yields the first column of the table.

Step 2) Compute response constants with (5) and derive f_n with (11). This gives the second part of the table.

Step 3) Compute peak voltage values and divide by V_{DC} to obtain the third part of the numerical tables.

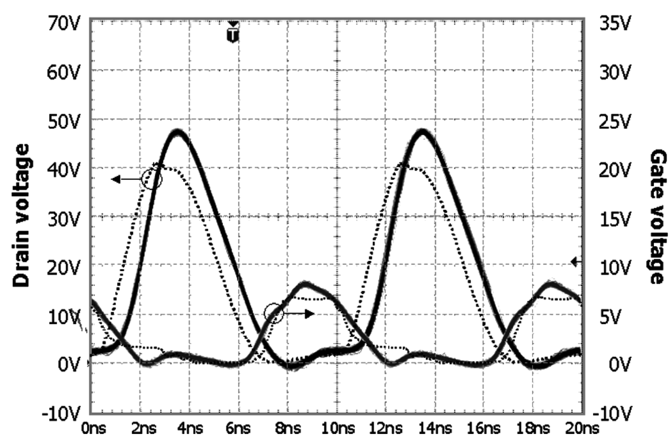


Fig. 9. Waveforms of drain voltage v_D and gate voltage in SPICE simulated (dotted line) and experimental (solid line) test circuit for the design example in Table III.

V. VERIFICATION

Three different procedures are investigated to verify this design method. The first one uses the particular results obtained in [4] to compare with a similarly specified design. In the second one, a circuit is designed and simulated in SPICE, and in the third case, the simulated circuit is built and tested to add experimental results to this paper, further proving the method.

A. Comparison With Other Analysis

In [4], an analytical method to design class E amplifiers with a combination of nonlinear and linear shunt capacitances is presented. The duty cycle is fixed to 0.5, as well as the grading coefficient $(n = 0.5)$, and the quality factor of the tuned output network is high, so, output is a sine wave. Making these particularizations in our design procedure and using similar specifications, the design values obtained (Table II) are exactly the same, except for the equivalent capacitance of the IRF510 transistor (something not calculated in [4]), which

TABLE IV
NUMERICAL RESULTS FOR DESIGN PROCEDURE FOR $Q_1 = 5$

$D = 0.25 \cdot Q_1 = 5 \cdot V_{bi} = 0.6 \cdot n = 0.3$																		
		$V_{DC}[V]$						$V_{DC}[V]$						$V_{DC}[V]$				
C_{eqn}		**1.5**	**3**	**6**	**12**	**24**	f_n	**1.5**	**3**	**6**	**12**	**24**	v_{Dpkn}	**1.5**	**3**	**6**	**12**	**24**
	0.1	0.539	0.47	0.398	0.314	0.264		0.006	0.007	0.008	0.009	0.011		2.481	2.557	2.565	2.457	2.464
	0.25	0.673	0.586	0.455	0.385	0.317		0.012	0.013	0.016	0.019	0.023		2.556	2.61	2.586	2.541	2.544
α	**0.50**	0.693	0.604	0.512	0.426	0.342		0.022	0.026	0.03	0.036	0.044		2.621	2.671	2.676	2.643	2.646
	0.75	0.739	0.644	0.546	0.43	0.348		0.031	0.036	0.043	0.051	0.062		2.748	2.802	2.816	2.715	2.751
	1	0.77	0.671	0.568	0.43	0.358		0.04	0.046	0.054	0.072	0.086		2.825	2.925	2.979	2.91	2.958
$D = 0.5 \cdot Q_1 = 5 \cdot V_{bi} = 0.6 \cdot n = 0.3$																		
		$V_{DC}[V]$						$V_{DC}[V]$						$V_{DC}[V]$				
C_{eqn}		**1.5**	**3**	**6**	**12**	**24**	f_n	**1.5**	**3**	**6**	**12**	**24**	v_{Dpkn}	**1.5**	**3**	**6**	**12**	**24**
	0.1	0.539	0.47	0.398	0.293	0.234		0.006	0.007	0.008	0.01	0.012		3.69	3.694	3.687	3.693	3.669
	0.25	0.673	0.482	0.4	0.361	0.298		0.012	0.014	0.017	0.02	0.024		3.78	3.702	3.713	3.723	3.724
α	**0.50**	0.647	0.584	0.485	0.392	0.333		0.024	0.027	0.032	0.039	0.047		3.786	3.779	3.785	3.785	3.824
	0.75	0.725	0.6	0.502	0.415	0.342		0.033	0.038	0.045	0.054	0.066		3.837	3.842	3.854	3.918	3.929
	1	0.725	0.611	0.515	0.427	0.355		0.045	0.054	0.064	0.077	0.093		3.915	3.952	3.984	4.115	4.147
$D = 0.75 \cdot Q_1 = 5 \cdot V_{bi} = 0.6 \cdot n = 0.3$																		
		$V_{DC}[V]$						$V_{DC}[V]$						$V_{DC}[V]$				
C_{eqn}		**1.5**	**3**	**6**	**12**	**24**	f_n	**1.5**	**3**	**6**	**12**	**24**	v_{Dpkn}	**1.5**	**3**	**6**	**12**	**24**
	0.1	0.145	0.143	0.125	0.088	0.075		0.001	0.001	0.002	0.002	0.002		7.259	7.242	7.238	7.216	7.22
	0.25	0.438	0.33	0.275	0.222	0.184		0.002	0.003	0.003	0.004	0.005		7.387	7.314	7.283	7.285	7.303
α	**0.50**	0.507	0.41	0.35	0.288	0.238		0.005	0.005	0.006	0.008	0.009		7.403	7.395	7.455	7.485	7.494
	0.75	0.535	0.446	0.37	0.309	0.253		0.007	0.008	0.009	0.011	0.013		7.546	7.572	7.628	7.645	7.668
	1	0.557	0.475	0.397	0.33	0.272		0.012	0.014	0.016	0.02	0.024		8.044	8.083	8.189	8.28	8.352
$D = 0.25 \cdot Q_1 = 5 \cdot V_{bi} = 0.6 \cdot n = 0.5$																		
		$V_{DC}[V]$						$V_{DC}[V]$						$V_{DC}[V]$				
C_{eqn}		**1.5**	**3**	**6**	**12**	**24**	f_n	**1.5**	**3**	**6**	**12**	**24**	v_{Dpkn}	**1.5**	**3**	**6**	**12**	**24**
	0.1	0.453	0.36	0.273	0.201	0.145		0.007	0.009	0.011	0.015	0.021		2.499	2.569	2.569	2.557	2.515
	0.25	0.565	0.449	0.341	0.251	0.173		0.014	0.017	0.023	0.031	0.043		2.596	2.65	2.654	2.645	2.569
α	**0.50**	0.582	0.463	0.351	0.245	0.181		0.027	0.033	0.044	0.06	0.083		2.713	2.771	2.782	2.769	2.812
	0.75	0.621	0.493	0.374	0.257	0.189		0.037	0.047	0.062	0.084	0.117		2.915	2.989	3.012	3.012	3.073
	1	0.646	0.506	0.368	0.258	0.192		0.048	0.061	0.084	0.12	0.161		3.102	3.2	3.155	3.375	3.492
$D = 0.5 \cdot Q_1 = 5 \cdot V_{bi} = 0.6 \cdot n = 0.5$																		
		$V_{DC}[V]$						$V_{DC}[V]$						$V_{DC}[V]$				
C_{eqn}		**1.5**	**3**	**6**	**12**	**24**	f_n	**1.5**	**3**	**6**	**12**	**24**	v_{Dpkn}	**1.5**	**3**	**6**	**12**	**24**
	0.1	0.453	0.276	0.182	0.168	0.129		0.007	0.009	0.012	0.016	0.023		3.703	3.692	3.698	3.706	3.716
	0.25	0.494	0.353	0.283	0.221	0.167		0.015	0.018	0.024	0.033	0.045		3.773	3.726	3.753	3.759	3.769
α	**0.50**	0.582	0.448	0.337	0.248	0.187		0.028	0.036	0.047	0.064	0.088		3.845	3.862	3.879	3.965	4.006
	0.75	0.621	0.47	0.348	0.263	0.194		0.04	0.05	0.066	0.09	0.124		3.987	4.007	4.025	4.224	4.276
	1	0.646	0.483	0.363	0.276	0.201		0.051	0.068	0.091	0.119	0.164		4.208	4.276	4.345	4.751	4.807
$D = 0.75 \cdot Q_1 = 5 \cdot V_{bi} = 0.6 \cdot n = 0.5$																		
		$V_{DC}[V]$						$V_{DC}[V]$						$V_{DC}[V]$				
C_{eqn}		**1.5**	**3**	**6**	**12**	**24**	f_n	**1.5**	**3**	**6**	**12**	**24**	v_{Dpkn}	**1.5**	**3**	**6**	**12**	**24**
	0.1	0.076	0.061	0.039	0.032	0.027		0.001	0.002	0.002	0.003	0.005		7.298	7.252	7.236	7.261	7.266
	0.25	0.262	0.18	0.136	0.112	0.083		0.003	0.004	0.005	0.006	0.009		7.381	7.338	7.319	7.388	7.398
α	**0.50**	0.358	0.265	0.197	0.15	0.111		0.006	0.007	0.009	0.013	0.017		7.516	7.542	7.579	7.647	7.69
	0.75	0.382	0.29	0.215	0.162	0.119		0.008	0.01	0.013	0.018	0.024		7.868	7.804	7.859	7.935	7.973
	1	0.404	0.316	0.236	0.174	0.127		0.016	0.021	0.027	0.037	0.051		8.874	9.142	9.413	9.661	9.804

was important to *a priori* determine the external capacitance value with precision. Peak voltage value, as well as output power and other performance parameters, are equal in both cases.

B. Simulated and Experimental Results

Fig. 8 shows the class E amplifier that has been designed with this method, simulated and built for $f = 100$ MHz, $D = 0.3$, and $Q = 5$, and output power of 1 W. Precise component values are shown in Table III. The device used is PolyFET's P123 LDMOS and the nonlinear dependence of $C_{\rm out}(v)$ has been extracted from datasheet information. In the design, the amplifier optimum load resistance was 24 Ω based on the method (theory) presented in this paper. A value of 16.2 Ω was obtained when performing SPICE simulations and experiments. The difference between theory and experiment is the inclusion of on resistance and component losses in the SPICE simulation [16]. The results have been simulated using SPICE. The circuit has been built and tested. The ZVS was achieved straight away at the desired 100-MHz frequency without any need of optimization loops in the design process. The expected efficiency (72.7%) is almost exactly achieved (71.4%) and could be improved with a lower on resistance device. Fig. 9 shows the results obtained in the simulation for the drain voltage waveform compared to the oscilloscope captured plot for the same waveform in the experiment. A specific D-variable driver has been designed and built for this purpose.

VI. Conclusion

In this paper, a novel and straightforward design method has been presented for class E amplifiers for any combination of nonlinear and linear capacitances shunting the device, duty cycle, output harmonic content, and possible nonlinear dependence. Losses in all the elements may also be included to predict the performance. The advantage of this method is that, to account for the nonlinearities, an equivalent linear capacitance is computed. This equivalent capacitance can be directly substituted in any other class E design method, except for a few parameters that need to be recalculated. Guidelines to calculate this capacitance are provided. Some representative results are summarized in graphs and additional results are presented in tables. To verify the method, three different alternatives have been tested, which are: 1) comparison with results of an existing less general analysis; 2) simulation, and 3) experimental verification; all of them yielding positive results.

Appendix
Numerical Results in Tables

In Table IV, an extensive set of numerical results for the design process are given. The data provided covers a good number of representative examples for three different values D, five possible values of α, eight possible values of supply voltage, and two possible values of n ($n = 0.3$ and $n = 0.5$) and for $V_{\rm bi} = 0.6$ and $Q_1 = 5$. These are only examples provided here for simplicity, but any particular combination of all the parameters mentioned previously can be numerically computed with this design procedure. The tables for $Q_1 = 2$ and $Q_1 = 10$ are directly obtainable from the authors upon request.

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References

[1] N. O. Sokal and A. D. Sokal, "Class E—A new class of high-efficiency tuned single-ended switching power amplifiers," *IEEE J. Solid-State Circuits*, vol. SC-10, no. 3, pp. 168–176, Jun. 1975.

[2] M. J. Chudobiak, "The use of parasitic nonlinear capacitors in class-E amplifiers," *IEEE Trans. Circuits Syst. I, Fundam. Theory and Appl.*, vol. 41, no. 10, pp. 941–944, Dec. 1994.

[3] T. Suetsugu and M. K. Kazimierckzuk, "Comparison of class-E amplifier with nonlinear and linear shunt capacitance," *IEEE Trans. Circuits Syst. I, Fundam. Theory and Appl.*, vol. 50, no. 8, pp. 1089–1097, Aug. 2003.

[4] ——, "Analysis and design of class-E amplifier with shunt capacitance composed of nonlinear and linear capacitances," *IEEE Trans. Circuits Syst. I, Fundam. Theory and Appl.*, vol. 51, no. 7, pp. 1261–1268, Jul. 2004.

[5] A. Mediano, "Contribution al estudio de los amplificadores de potencia de RF clase E. influencia de la capacidad de salida del dispositive active," (in Spanish) Ph.D. dissertation, Dept. Electron. Commun. Eng., Univ. Zaragoza, Zaragoza, Spain, 1997.

[6] C. Chan and C. Toumazou, "Design of class-E power amplifier with nonlinear transistor output capacitance and finite DC feed inductance," in *Int Circuits Syst. Symp.*, Sydney, Australia, Jun. 2001, pp. 1129–1132.

[7] P. Alinikula, D. K. Choi, and S. Long, "Design of class-E power amplifier with nonlinear parasitic capacitance," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 46, no. 2, pp. 114–119, Feb. 1999.

[8] N. O. Sokal and R. Redl, "Power transistor output port model," *RF Des.*, vol. 10, pp. 45–48, Jun. 1987.

[9] A. Mediano, P. Molina, and J. Navarro, "Class E RF/microwave power amplifier: Linear 'equivalent' of transistor's nonlinear output capacitance, normalized design and maximum operating frequency vs. output capacitance," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Boston, MA, 2000, pp. 783–786.

[10] P. Molina-Gaudo, C. Bernal, and A. Mediano, "Design technique for class E RF/MW amplifiers with linear equivalent of transistor's output capacitance," in *Proc. IEEE Asia–Pacific Microw. Conf.*, Dec. 2005, vol. 2, 4 pp.

[11] A. Mediano and P. Molina, "Frequency limitation of a high-efficiency class E tuned power amplifier due to a shunt capacitance," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 1999, pp. 363–366.

[12] J. M. Burdío and A. Martinez, "A unified discrete-time state-space model for switching converters," *IEEE Trans. Power Electron.*, vol. 10, no. 6, pp. 694–707, Nov. 1995.

[13] M. Kazimierczuk and K. Puczko, "Exact analysis of a class E tuned power amplifier at any Q and switch duty cycle," *IEEE Trans. Circuits Syst.*, vol. CAS-34, no. 2, pp. 149–159, Feb. 1987.

[14] P. Molina-Gaudo, "A contribution to nonlinear class-E amplifier device modelling and parameter extraction," Ph.D. dissertation, Dept. Electron. Commun. Eng., Univ. Zaragoza, Zaragoza, Spain, 2004.

[15] D. Kessler and M. K. Kazimierckzuk, "Power losses and efficiency of class E power amplifier at any duty ratio," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 51, no. 9, pp. 1675–1689, Dec. 1996.

[16] N. Sokal, "Class E RF power amplifiers," *QEX/Commun. Quarterly Mag.*, vol. 46, no. 12, pp. 2220–2225, Jan./Feb. 2001.

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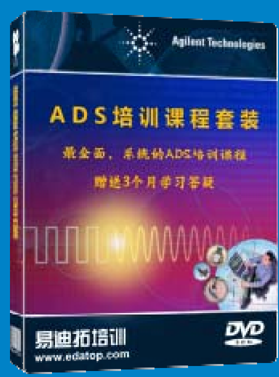

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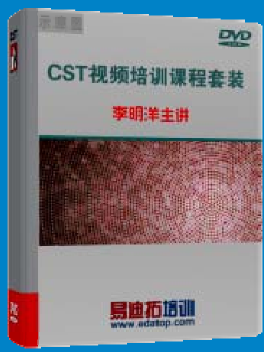

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